Modicon TSX Quantum

140 EHC 105 00
High Speed Counter Module
User Manual

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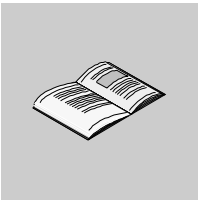
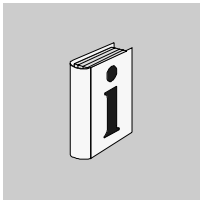
Table of Contents



About the book



At a Glance

Document Scope

This User Manual, including the EHC 105 module description, is to serve as an aid to fast counter configuration.

- The operational characteristics of the EHC 105
- The module configuration and parameterization
- The module description EHC 105
- The configuration examples
- The EHC 105 derived data types

Validity Note

The primary basis of this documentation is the EHC 105 module HW index level 12.02 and firmware version 2.0.7. The corresponding configuration software is Concept >= Release 2.1 under Microsoft NT/98/2000 or Modsoft >= Release 2.4 under Microsoft Windows NT/95.

Note: The latest information can be found in the Concept README file.

Related Documents

Title of Documentation	Reference Number
Modicon TSX Quantum Automation Series, Hardware Reference Guide	840 USE 100 00
Modbus Plus Network, User's Manual	890 USE 100 02
Modicon Modlink, User's Guide	GM-MLNK-001
Modicon IBM Host Based Devices, User's Guide	GM-HBDS-001
BM85 Modbus Plus Bridge / Multiplexer, User's Guide	GM-BM85-001

User Comments We welcome your comments about this document. You can reach us by e-mail at TECHCOMM@modicon.com

EHC 105 00 Functional Overview

I

At a Glance

Introduction

This part includes information about functionality of the High Speed Counter EHC 105 00 module.

What's in this part?

This Part contains the following Chapters:

EHC 105 00 Introduction

1

At a Glance

Introduction

This chapter includes information about global functionality of the High Speed Counter EHC 105 00 module.

What's in this Chapter?

This Chapter contains the following Maps:

General User Characteristics for EHC 105 00

User Characteristics

The user characteristics are presented below:

- The EHC 105 00 module is a high-speed counter module for the Modicon TSX Quantum controller.
- The EHC 105 00 includes 5 independent counters.
- Each counter can be operated with either 5 or 24 VDC pulse input signals.
- The counters can be operated in the following operating modes:
  - Event counter, 32-bit, with four distinct operating modes
  - Differential counter, 32-bit, with two distinct operating modes
  - Repetitive counter, 16-bit
  - Rate counter, 32-bit, with two distinct operating modes
- Counting frequencies of up to 100 kHz can be monitored, depending upon cable length, transmitter type and voltage refer to *EHC 105 00 Hardware Specifics, p. 76*.
- There are eight isolated, discrete inputs and eight isolated, discrete outputs (24 VDC level) available. These discrete I/Os can be assigned to the various signals of the individual counters.

System Characteristics of EHC 105 00

System Characteristics

EHC 105 is characterized by the following features:

- The EHC 105 00 is used with Concept.
- Configuration information is transferred from the controller to the EHC 105 00 module only at controller start up or module hot swap.
- Data transfer of the set point and actual values is exchanged every scan cycle.
- The user program is processed in the controller.
- The EHC105 module functions asynchronously with the controller, allowing fast response and control.

Note: Certain parameter defaults are assigned at module start-up, which among other things, assign specific functions to the discrete inputs (refer to *Overview of I/O Signals , p. 18*).

Menu Selection of Terms

Concept 2.0

The following terms of Concept Version 2.0 menus are:

- **Output switch-off**
- **Preceded signal**
- **Preceded set point**
- **Final signal**
- **Final signal value**
- **Dynamic final signal**
- **Clock watchdog time**
- **Clock enable**
- **Invert clock**

Concept 2.1

The following terms of Concept Version 2.1 menus are:

- **Output switch-off**
- **Set point**
- **Output set point**
- **Final set point**
- **Final set point value**
- **Timed final set point**
- **Counter watchdog time**
- **Counter enable**
- **Input signal counts on**
  - **Pos. Transition**
  - **Neg. Transition**

Configuration with Concept

For configuration, Concept offers five dialog screens.

Structural Description of EHC 105 00

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At a Glance

Introduction

This chapter describes the hardware configuration and the structure of the EHC 105 00 module.

What's in this Chapter?

This Chapter contains the following Maps:

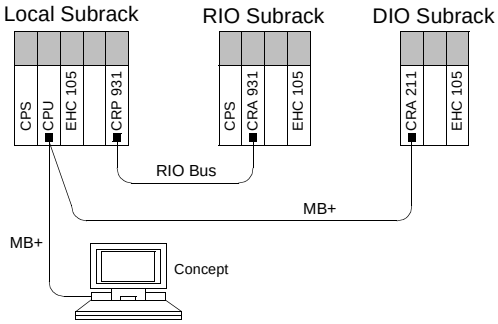
Hardware Configuration of EHC 105 00

Hardware Configuration

The counter module can be mounted in:

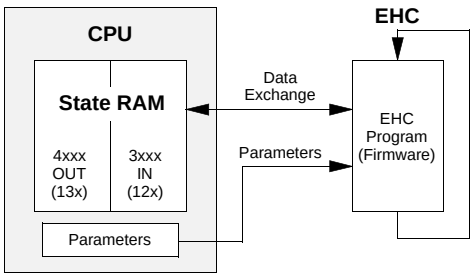
- Local subrack
- RIO subrack
- DIO subrack

A typical hardware configuration is shown below.



State RAM Diagram

The counter module needs 13 OUT (4x...) and 12 IN registers for configuration. The state RAM diagram as used by the counter is shown in the figure below.



Block Diagram of a Counter Channel

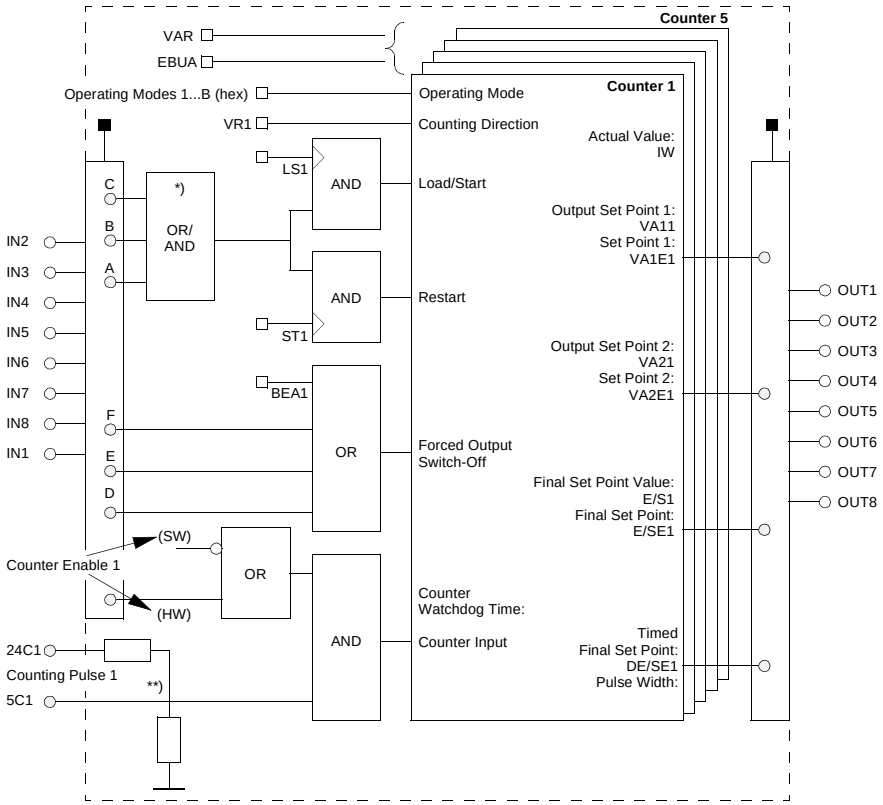
Parts of a Counter Channel

Each counter channel consists of the following parts:

- Discrete input signals
- Input logic
- Input functionalities
- Output functionalities
- Output signals

Block Diagram

Block diagram of a counter channel



Meaning of the symbols inside the graphic:

Symbol	Meaning
*)	Configurable as either AND or OR. If the gate is not configured the output from this gate is TRUE.
**)	The counting pulse input voltage divider has been schematically simplified
○—	Discrete input signals
—○	Discete output signals
□—	State RAM
—○|	Inversion
——	Parameter from the Concept/Modsoft configuration dialog
■	Discrete IN/OUT assignments to the internal counter signals and possible I/O inversions (through a configuration dialog)

Overview of I/O Signals

Overview

Overview of I/O signals and parameters.

Signal	Description
IN1 ... 8:	Discrete input signals which can be connected and individually inverted to the counter's control inputs.
24Cx/5Cx (x = 1...5):	Discrete inputs for 24/5 VDC counting pulses.
VAR:	Bit within an output register (4x...), which determines if the output set points will be relative or absolute to final set point value for all 5 counters.
EBUA:	Output register (4x...) bit, which determines module switch-off behavior for all 5 counters when communication between the controller and EHC 105 00 is interrupted.
Operating modes 1...B:	One of 11 possible operating modes that can be selected for each counter through a 4x register.
VRx (x = 1...5):	Bit within an output register (4x...), which determines the counting direction.
LSx (x = 1...5):	Load/Start: Bit within an output register (4x...), minimum pulse width: 3 ms.
BEAx (x = 1...5):	Output switch-off: Bit within an output register (4x...). The pulse must be at least 3ms width.
STx (x = 1...5):	Counter restart: Bit within an output register (4x...), minimum pulse width: 3 ms.
Counter enablex:	There are two different enable inputs for every counter: • Software Counter enable • Hardware Counter enable
Counter watchdog timer:	This timer monitors incoming pulses.
VA1x (x = 1...5):	The first output set point.
VA1Ex (x = 1...5):	First set point: Bit within an input register (3x...) to control the counter.
VA2x (x = 1...5):	Second output set point.
VA2Ex (x = 1...5):	Second set point: Bit within an input register (3x...) to control the counter.
E/Sx (x = 1...5):	Final set point value: Output register (4x...).
E/SEx (x = 1...5):	Final set point: Bit within an input register (3x...).

Signal	Description
DE/SEx (x = 1...5):	Timed final set point: Settable through the Concept dialog screen.
Pulse width:	Defines the length of the timed final set point pulse. In operating mode A: Defines the time for all associated outputs.
OUT1...8:	Discrete output signals, which can be assigned and individually inverted to the counter output.

Operational Characteristics of EHC 105 00

3

At a Glance

Introduction

This chapter includes detail information about the operational characteristics of the EHC 105 00 module.

What's in this Chapter?

This Chapter contains the following Maps:

Discrete I/O Signals

IN1...IN8

IN1 ... IN8 are discrete input signals which can be connected and individually inverted to the counter's control inputs

Response Times

The response times (including firmware scans) are :
- 10 ms for IN1...IN6
- 5 ms for IN7 and IN8

Rules

The following rules apply to IN1...IN8:
- Each INx signal may be selected several times.
- Every input may be assigned the load/start, restart, or forced output switch-off functions.
- Inputs can also be used as counter enable. However in this case the allocations are defined and may not be changed (IN1 is allocated counter 1, IN2 to counter 2, and so on.).
- Each discrete input can be inverted through the configuration dialogs.

Default

- The default for IN1...IN8 is **Not inverted**.
- For default assignment refer to *Start-Up Characteristics, p. 69*.

24Cx/5Cx (x=1...5)

24Cx/5Cx (x = 1...5) are discrete inputs for 24/5 VDC counting pulses.

Counting on Pos. or Neg. Transition

Every counter has it´s own counting pulse inputs.
You have the following choice for configuration of the counter:

If Input Signal counts on: ...	**Then the counter will count on the ...**
Is not selected (**Invert clock** in Concept 2.0)	**Neg. Transition**
Is selected	**Pos. Transition**

The default is **Neg. Transition**.

OUT1...OUT8

OUT1 ... OUT8 are discrete output signals, which can be assigned and individually inverted to the counter outputs VA1E (set point 1), VA2E (set point 2), E/SE (final set point), and DE/SE (timed final set point).

Default

- The outputs OUT1...OUT8 are not inverted.
- The default assignment refer to *Start-Up Characteristics, p. 69*.

	**WARNING**
	Risk of unpredictable process states Do not select the same output OUT1 ... OUT8 with more than one set point. Such double assignments lead to unpredictable process states, and are particularly difficult to diagnose. **Failure to observe this precaution can result in severe injury or equipment damage.**

Functional Counter Features

Overview

The possible settings relating to the functional features of the five counters in your EHC 105 are described in the following. The figure below illustrates the setting possibilities.

Output Set Points

For all five counters the bit VAR determines if the output set points will be relative or absolute to final set point value. VAR is a bit within an output register (4x...).
The signal signification of VAR is:

- VAR = 1: output set point is relative (to the final set point value).
- VAR = 0: output set point is absolute.

Default setting for VAR before configuration is VAR = 0.
See also *Output Set Point Mode, p. 32*.

Module Switch-Off Behaviour

The module switch-off behavior for all five counters when communication between the controller and EHC 105 00 is interrupted is determined by EBUA. EBUA is an output register (4x...) bit.
The signal signification of EBUA is:

- EBUA = 1: The current output state is retained.
- EBUA = 0: All used outputs are set to 0 level.

Operation Modes

The operation mode of each of the five counters is determined by the value of BA. BA is a 4x register, which can take one of 11 values (1....9, A, B), each representing a specific operation mode. For the meaning of the values 1 ... B refer to *Mode Number of Counter Types, p. 39*.
Before configuration, the default mode of all counters is equivalent to operating mode A. The modes named 0, C, D, E, F are equal to the mode A.

Counting Direction

The individual counters can function as bidirectional counters, counting up or down. The counting direction of each counter is determined by VRx (x = 1...5).
VRx (x = 1...5) is a bit within an output register (4x...).
The signal signification of VRx (x = 1...5) is:

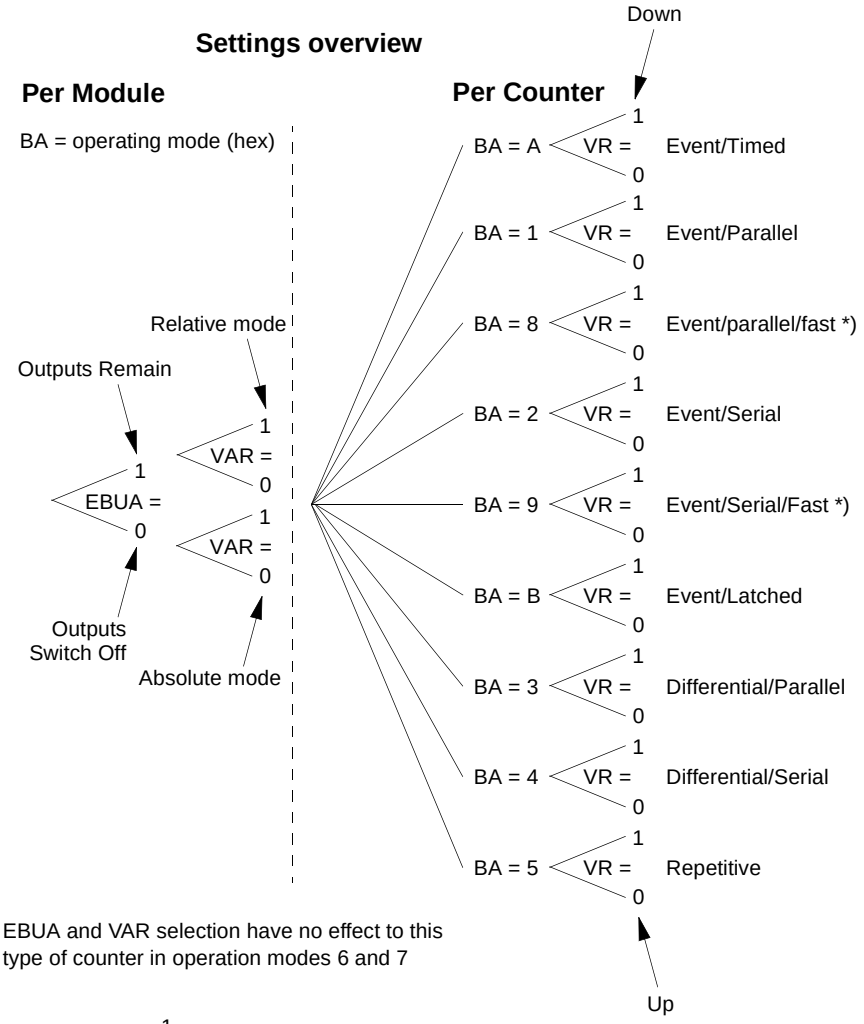
- VRx = 0: Up-counter, starting with 0, stop at final value E/Sx.
- VRx = 1: Down-counter, starting at initial value E/Sx, stop at 0.

Note: Do not change the value of the VRx bit during operation of the counter. If the value changes, the associated outputs of the counter will be switched off.

Before configuration, the default value for VRx is VRx (x = 1...5) = 0.

Counter Settings for Functional Features

Possible counter settings determining the functional features of the five counters are presented below:



***)** Fast counters have no restart function

Start and Stop Counter Functionality

Load / Start

Load/start, LSx (x = 1...5), is a bit within an output register (4x...), minimum pulse width: 3 ms.
For more information refer to *Start and Stop Time Diagram without Hardware Input Configuration, p. 27* and *Start and Stop Time Diagram with Hardware Input Configuration, p. 29*.
Default value before configuration is LSx (x = 1...5) = 0.

Output Switch-Off

Output switch-off, BEAx (x = 1...5), is a bit within an output register (4x...). The pulse must be at least 3 ms width.
If BEAx = 1, it latches the current count in a buffer. While the counter continues to count, VA1Ex, VA2Ex and E/SEx are reset. This is also true for any assigned outputs OUTx.
For more information refer to *Start and Stop Time Diagram without Hardware Input Configuration, p. 27* and *Start and Stop Time Diagram with Hardware Input Configuration, p. 29*
Default value before configuration is BEAx (x = 1...5) = 0.

Restart

Counter restart, STx (x = 1...5), is a bit within an output register (4x...), minimum pulse width: 3 ms.
The STx signal releases the buffer and counter values of equal current value.
For more information refer to *Start and Stop Time Diagram without Hardware Input Configuration, p. 27* and *Start and Stop Time Diagram with Hardware Input Configuration, p. 29*
Default value before configuration is STx (x = 1...5) = 0.

Start and Stop Priority Ranking of Signals

Priority Ranking

The priority of signals to start or stop a counter is as follows:

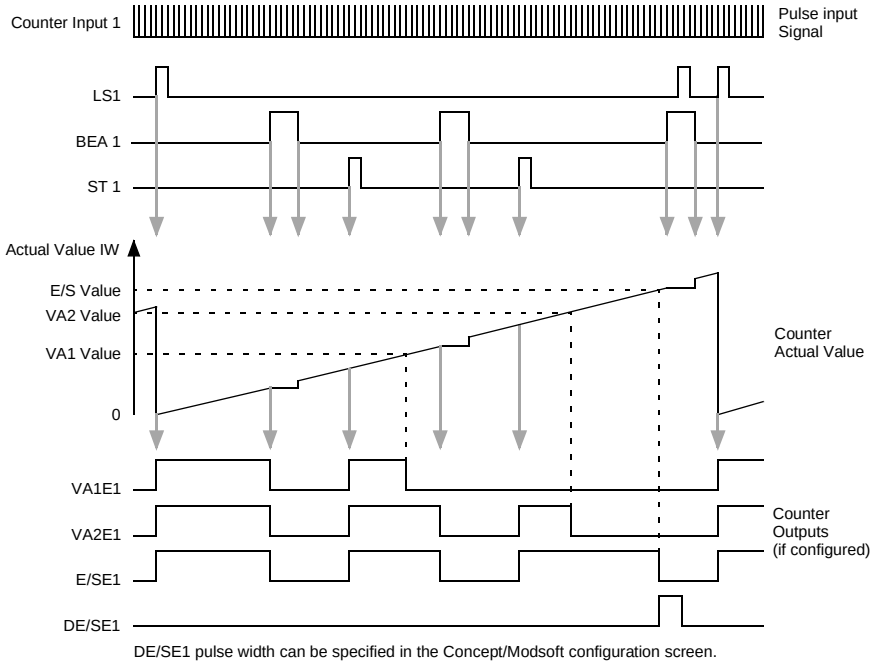
Priority	Function	Active for:
1	Forced output switch-off	BEAx = 1 (state RAM) or One of the configured discrete inputs is 1.
2	Load/Start counter	LSx = 1 (state RAM) and TRUE evaluation of the configured discrete inputs
3	Restart counter	STx = 1 (state RAM) and TRUE evaluation of the configured discrete inputs

Note: The user program commands are necessary for starting and restarting of the counting procedures. Setting of the corresponding discrete inputs is also required. When no discrete input is assigned to the commands through **Load/Start** and **Restart**, the counting procedure is initiated through the output status word (4x...) bits LSx respectively STx.

Start and Stop Time Diagram without Hardware Input Configuration

Time Diagram

The following time diagram shows the start and stop functionality without using the input signals load/start, restart, output switch-off and counter enable. Counter 1 is configured as event counter, parallel, absolute, output function non inverted and counting up.



DE/SE1 pulse width can be specified in the Concept/Modsoft configuration screen.

Influence of LS1

With the rising edge from LS1, the actual counting value is set to 0. The outputs VA1E1, VA2E1 and E/SE1 are set to 1 for the operation mode 1 ... 5 and 8, 9 or to 0 for operation mode A and B.

Influence of BEA1 and ST1

If BEA1 = 1 the actual value will latch; the counting continues in an internal memory of the module.
If BEA1 = 0 the counting of the actual value continues with the current contents of the memory. Is there on ST1 a rising edge the outputs switch on depending on the actual value.

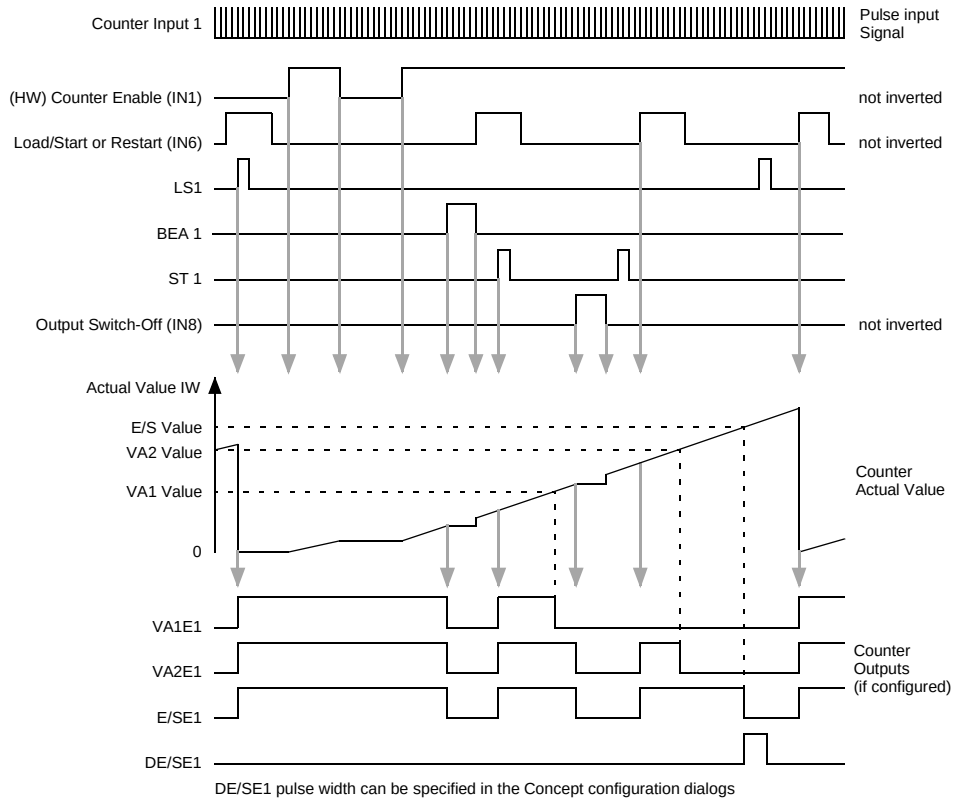
Note: Notice following notes:

- In mode 5, 8, 9 an 1 signal at BEA is setting the actual value to 0 or to final set point value, depending on up or down counting mode.
- The ST1 signal has no function in the modes 5, 8 and 9.

Start and Stop Time Diagram with Hardware Input Configuration

Time Diagram

The following time diagram shows the start and stop functionality with using the input signals load/start, restart, output switch-off and counter enable. Counter 1 diagram as event counter, parallel, absolute, output function non inverted and counting up.



DE/SE1 pulse width can be specified in the Concept configuration dialogs

Load/Start or Restart

- The discrete input evaluation for **Load/Start or Restart** is combined with LSx respectively STx by AND.
- The AND condition is true if no configuration has been carried out for **Load/Start or Restart**; the LSx and STx bits then function alone.

Influence of LSx and STx

- The LSx and STx signals operate edge-controlled.
- LSx and STx bit are always active with the rising ege, it can not be inverted.

Influence of BEAx

- BEAx is always active with the high signal, it can not be inverted.
- An active BEAx signal set all inverted outputs to high signal.

Discrete I/O

- If the discrete outputs are inverted, the state from the signals VA1Ex, VA2Ex and E/SEx will not be inverted.
- If the discrete input is not inverted, the high signal is active. If discrete input is inverted, the low signal is active.

Output-Switch-Off

- The output switch-off discrete inputs have the same function as the BEAx bit.

Further Signals

DE/SE pulse width can be specified in the Concept dialog screen.

Counter Enabling and Monitoring

SW counter enable 1-5

The software switch enables the counter and is activated from the Concept configuration screen. In the screen select the option as follows:

Option	Meaning
Input x for counter enable: is selected	The (HW) counter enable is effective.
Input x for counter enable: is not selected	The counting pulse is always enabled.

The default is **Input x for counter enable: is not selected** .

Note: The pulse counting begins after the first complete pulse following the counter enable signal. Accordingly, after counting pulse disable, the next counting pulse will still be registered. As a result during each count cycle (enable / disable), one pulse will be missing.

HW counter enable 1-5

Signal that enables the counter, if **Input x for counter enable** is selected. Input channels for this function are predefined:

Input	Counter
IN1	1
IN2	2
:	:

The signal signification for the (HW) counter enable is:

Signal	Meaning
1	Counter is enabled (input not inverted)
0	Counter is disabled (input not inverted)

The default: Input (HW counter) is not selectable for counter enable.

Note: The pulse counting begins after the first complete pulse following the counter enable signal. Accordingly, after counting pulse disable, the next counting pulse will still be registered. As a result during each count cycle (enable / disable), one pulse will be missing.

Counter Watchdog Timer

This timer monitors incoming pulses and can be enabled through the Concept dialog screen:
The parameter signification is:

- Value 0: no monitoring
- Values 1...255: (x 0.1) sec.

The default is value 0.

Output Set Point Mode

Output Set Point

There are two output set points per EHC module:
- The first output set point VA1x (x = 1...5)
- The second output set point VA2x (x = 1...5)

The output set point is configured once for all module counters. All counters of one module operate in absolute or relative output set point mode.
Value range of VA1x = 0...(2 exp31) 1
The default is value 0.

Output Set Point Modes

Signification and requirements of the output set points modes relative and absolute:

Output set point mode	Description	Requirement
Absolute	In this mode, the value entered in the Concept screen is the actual output set point.	E/Sx > VA2x >=VA1x >=0 E/Sx = final set point value
Relative	In this mode, the output set point is the difference between the entered value in the Concept screen and the final set point value.	E/Sx > VA1x >=VA2x >=0 E/Sx = final set point value

Set Points

Set Points

There are two set points per counter:
- VA1Ex (x = 1...5)
- VA2E (x = 1...5)

VA1Ex and VA2x are bits within an input register (3x..).
They may be assigned to any of the discrete outputs OUT1...OUT8.
Default: VA1Ex (x = 1...5) = 0 and VA1Ex (x = 1...5) = 0.
For default assignments refer to *Start-Up Characteristics, p. 69*.

Final Set Point Value

The final set point value E/Sx (x = 1...5) is an output register (4x...) in which the counter's final value (up counter) or inital value (down counter) is entered.
A change of the final set point value has the following effects:

Mode	Effects
1, 2, 3, 4	A change of the final set point value will be excepted immediately (independent if the counter is active or inactive). The actual value will not be influenced.
5	A change of the final set point value only takes effect if the BEA signal is set in advance.
8, 9	A change of this value has no effect, if the counter is active. If the counter is inactive a change of this value is excepted immediately.The actual value is setting to 0 or to final set point value, depending on up or down counting mode.

Value range: E/Sx (x = 1...5) = 0...(2 exp31) -1
Default value: E/Sx (x = 1...5) = 0

Final Set Point

The final set point E/SEx (x = 1...5) is a bit within an input register (3x...).
It may be assigned through the Concept dialog screen to any of the discrete outputs OUT1...OUT8.
Default value: E/SEx (x = 1...5) = 0.
For default assignments refer to *Start-Up Characteristics, p. 69*.

Timed Final Set Point

The timed final set point DE/SEx (x = 1...5) is settable through the Concept dialog screen. It can be assigned to any of the discrete outputs OUT1...OUT8.
Default value: DE/SEx (x = 1...5) = 0.
Default assignement is: No assignement.

Pulse Width

Pulse width defines the length of the timed final set point pulse. In addition, in operating mode A, pulse width defines the time for all associated outputs.
Significance of the pulse width value:

Pulse width value	Significance
0	Output for DE/SEx is disabled.
1...255	x = 0.02 sec

Default: Pulse width = 0.

Note: If pulse width = 0 in operating mode A there will be no outputs.

EHC 105 00 Counter Types and their Operating Modes

4

At a Glance

Introduction

This chapter includes information about the different Counter types and their possible operating modes.

What's in this Chapter?

This Chapter contains the following Sections:

4.1 Overview of Counter Types and their Mode Numbers

Overview

Introduction

This section describes the counter types and their mode numbers.

What's in this Section?

This Section contains the following Maps:

Overview of Counter Types

Counter Types

The EHC 105 00 module can operate as the following counter types:

- Event counter (with and without fast final set point)
- Event counter with timed or latched outputs
- Differential counter (without fast final set point)
- Repetitive counter (with fast final set point)
- Rate counter

Counting up and down

The selection of the various counter types takes place through the operating mode selections in state RAM. Every counter type can count up and down. Output set point mode can be set to be relative (to the Final Set Point Value) or absolute.

Reason for Switch-Off

For an active counter, any of the following changes triggers an output switch-off:

- Change of operating mode
- Change of counting direction
- Change of switch-off behavior
- Change of type of Set Point

Note: A change of the operating mode accompanied by load/start is not possible. The setting of the load / start bit after changing the operation mode must be done in the next scan cycle.

Discrete Output Signal Response Times

The response times for discrete output signals:

Set Point	Discrete output signal response time
Without fast final set point	Typically 3 ms
With fast final set point	Typically 0,5 ms

Mode Number of Counter Types

Counter Operating Mode Number

Counter operating and their mode number (hex).

Value (hex)	Meaning
1	Event counter with parallel Set Point activations.
2	Event counter with serial Set Point activations.
3	Differential counter with parallel Set Point activations (only applies to counters 1 and 3, the Set Point and actual values of counters 2 resp. 4 are inactive).
4	Differential counter with serial Set Point activations (only applies to counters 1 and 3, the Set Point and actual values of counters 2 resp. 4 are inactive).
5	Repetitive counter
6	Rate counter, gate time t = 100 ms
7	Rate counter, gate time t = 1 s
8	Event counter with parallel Set Point activations and fast Final Set Point.
9	Event counter with serial Set Point activations and fast Final Set Point.
A (default)	Event counter with timed "on" outputs, the pulse width setting holds for all employed outputs.
B	Event counter with latched Set Point outputs.
0, C, D, E, F	As operating mode A.

4.2 Event Counter

Overview

Introduction

This section describes the operating modes of EHC 105 if it is working as an event counter.

What's in this Section?

This Section contains the following Maps:

Operating Modes

Characterization

The event counter is a gate-controlled, bidirectional counter with two or less set points, a final set point and a timed final set point.

Operating Modes

The event counter has the following operating modes:

Operating Mode	Description
A	With adjustable "time on" outputs. The pulse width configuation applies the same value to all counter outputs.
1	With parallel output set point activation.
2	With serial output set point activation.
8	With parallel output set point activation and fast final set point.
9	With serial output set point activation and fast final set point.
B	With latched set point activation.

Note: Outputs are at "0" signal on start.

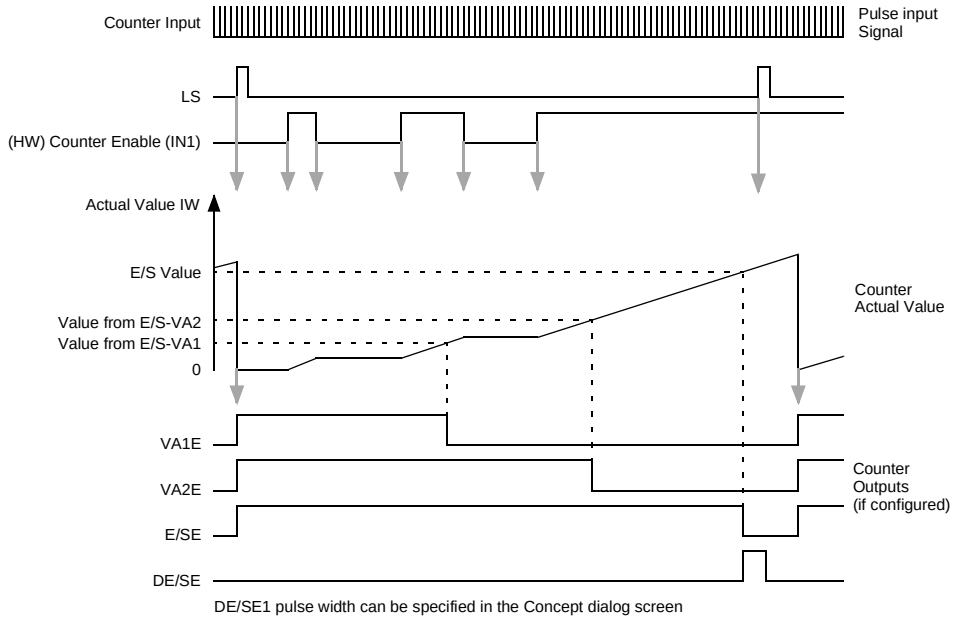
Value Range

The value range for all operating modes amounts to: 0...(2 exp 31) 1, except the operating mode 5 is 0...(2 exp 16) 1.

Time Diagrams for Operating Modes 1 and 8

Counting up

Counting up is realised with VRx = 0.



Further Signals

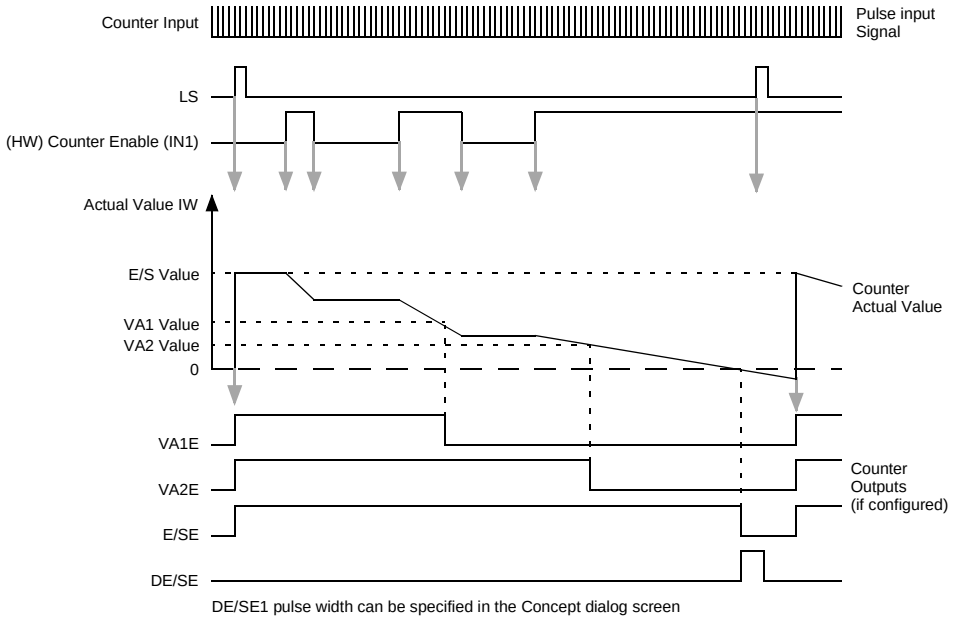
DE/SE pulse width can be specified in the Concept dialog screen.
This event counter with relative and serial set point activation is a typical time diagram that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality , p. 26*
- STx: Further information see *Start and Stop Counter Functionality , p. 26*

Note: STx has no function in the operating mode 8.

Counting down Counter

Counting down is realised with VRx = 1.



Further Signals

DE/SE pulse width can be specified in the Concept dialog screen.
This event counter with relative and serial set point activation is a typical time diagram that does not take into account the following signals:

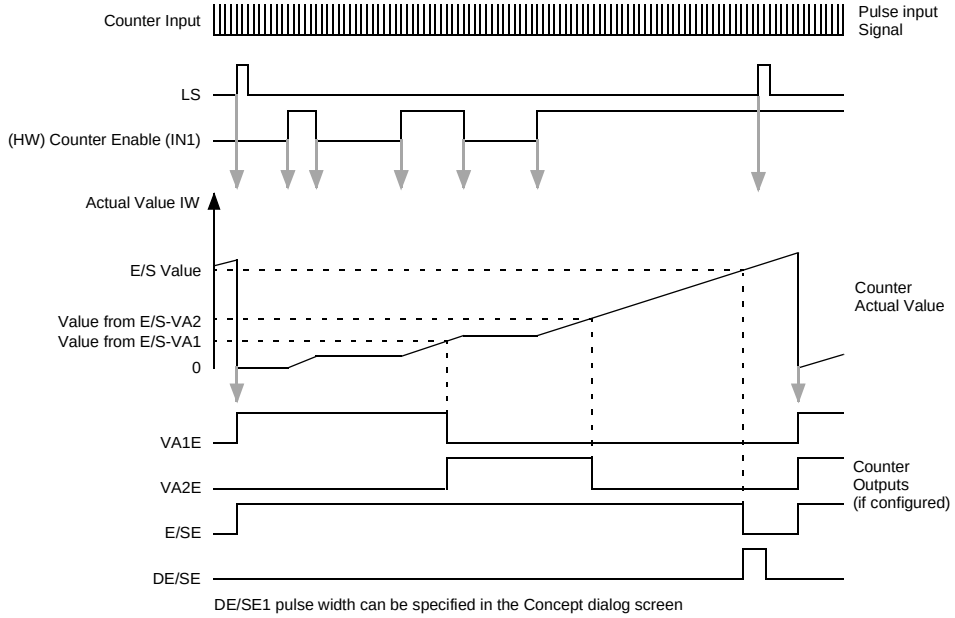
- BEAx: Further information see *Start and Stop Counter Functionality , p. 26*
- STx: Further information see *Start and Stop Counter Functionality , p. 26*

Note: STx has no function in the operating modes 8.

Time Diagram for Operating Modes 2 and 9

Counting up

Counting up is realised with VRx = 0.



Further Signals

DE/SE pulse width can be specified in the Concept dialog screen.
This event counter with relative and serial set point activation is a typical time diagram that do not take into account the following signals:

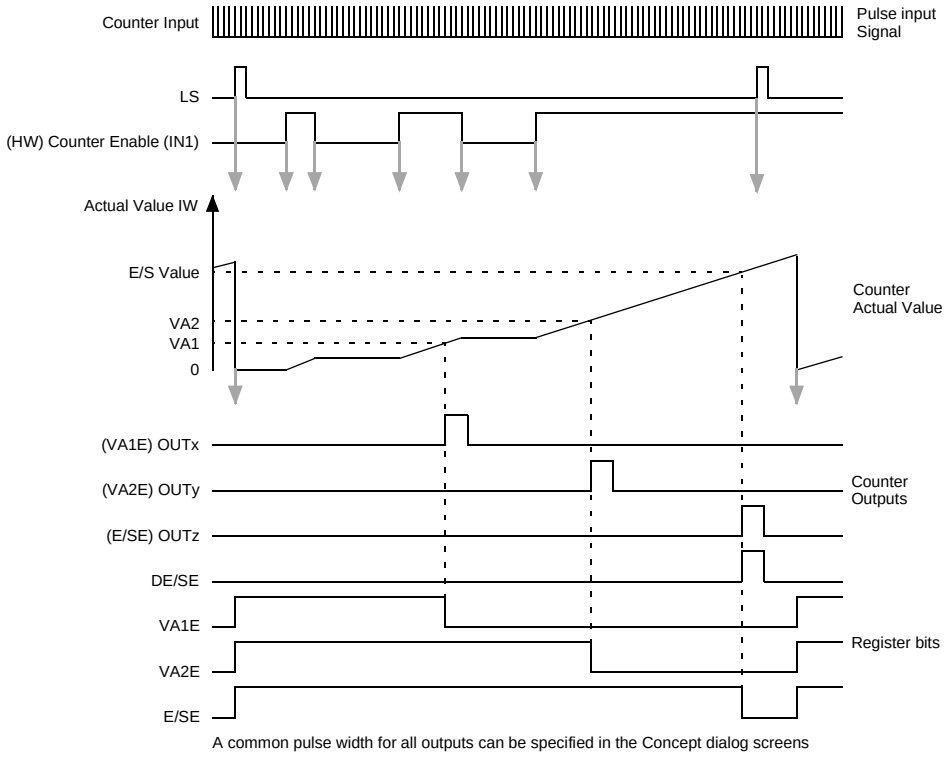
- BEAx: Further information see *Start and Stop Counter Functionality , p. 26*
- STx: Further information see *Start and Stop Counter Functionality , p. 26*

Note: STx has no function in the operating mode 9.

Time Diagram for Operating Mode A

Counting up

Counting up is realised with VRx = 0.



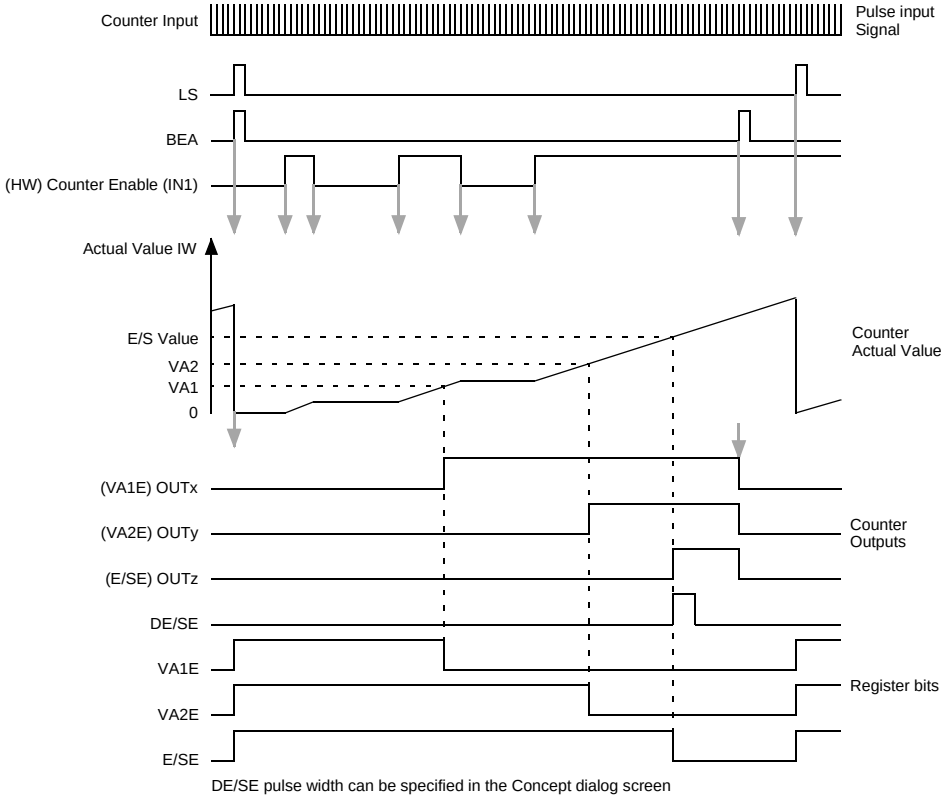
DE/SE pulse width can be specified in the Concept dialog screen.

Note: The activation of the discrete outputs are different from the activation of the register bits.

Time Diagram for Operating Mode B

Counting up

Counting up is realised with VRx = 0.



DE/SE pulse width can be specified in the Concept dialog screen.

Note: The activation of the discrete outputs are different from the activation of the register bits.

4.3 Differential Counter

Overview

Introduction

This section describes the operating modes of EHC 105 if it is working as a differential counter.

What's in this Section?

This Section contains the following Maps:

Operating Modes

Characterization

The differential counter is a gate-controlled counter with up to two output set points, a final set point and a timed final set point. A differential counter consists of two counter channels and measures the difference of each of their pulses.
The counting value is determined from the difference of the two counters.
Counter 1 (clockwise) and 2 (counterclockwise) form a differential counter 1, while counter 3 (clockwise) and 4 (counterclockwise) form a differential counter 2.

Note: This configuration cannot be changed.

Operating Modes

The differential counter has the following operating modes:

Operating Mode	Description
3	With parallel set point activation.
4	With serial set point activation.

Note: Outputs are at "0" signal on start.

Configuration Note

Differential counter configuration, control and evaluation is done through the parameters and values of the first counter with the exception of the counter input.
The configuration for the respective second counter must be performed separately.
The parameter choices (from the Concept dialog screen) are:

- **Invert counter input / input signal counts on**
- **Use input for counter enable / input for counter enable**

Note: A fast final set point cannot be set for differential counters. If a counter is disabled, counter time monitoring is suspended.

Value Range

The value ranges are as follows:

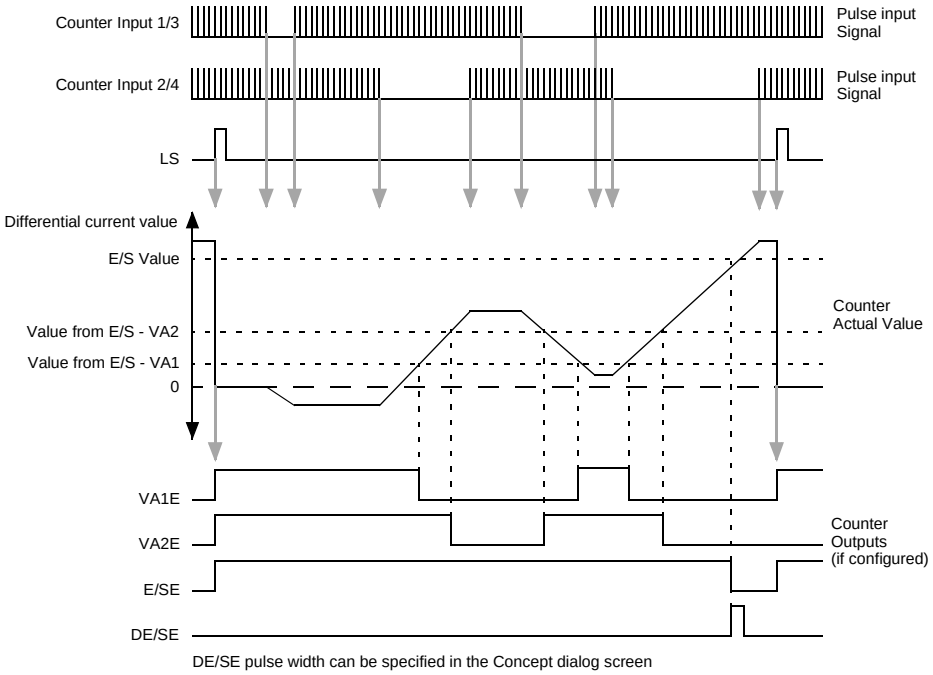
- Set Point values: 0...(2 exp 30) -1.
- Actual values: -(2 exp 30)...(2 exp 30) -1.

Note: The value range allows the differential counter to be used also for continuous monitoring.

Time Diagram for Operating Mode 3

Counting up

Counting up is realised with VRx = 0.

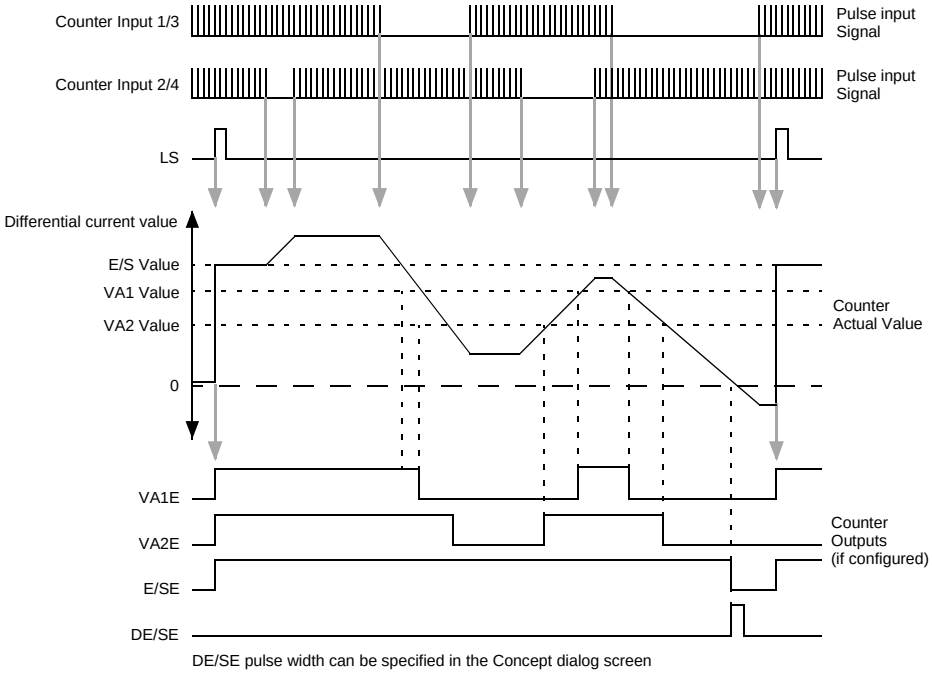


Further Signals

DE/SE pulse width can be specified in the Concept dialog screen.
This differential counter with parallel set point cutoffs is a typical time diagram that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality , p. 26*
- STx: Further information see *Start and Stop Counter Functionality , p. 26*

Counting down Counting down is realised with VRx = 1.



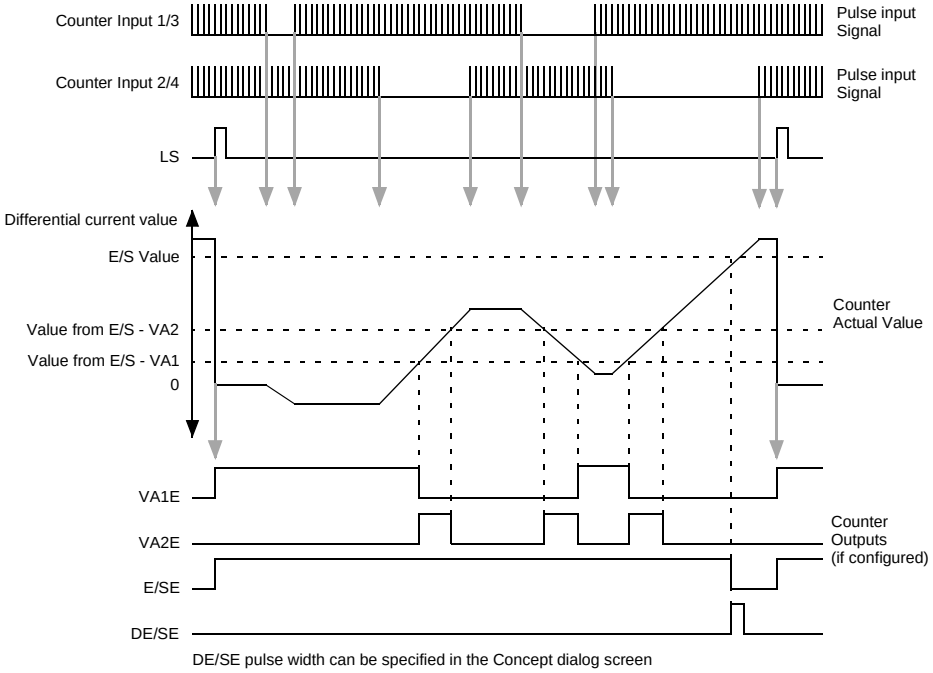
Further Signals This differential counter with parallel set point cutoffs is a typical time diagram that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality , p. 26*
- STx: Further information see *Start and Stop Counter Functionality , p. 26*

Time Diagram for Operating Mode 4

Counting up

Counting up is realised with VRx = 0.



Further Signals

DE/SE pulse width can be specified in the Concept dialog screen.
This differential counter with seriall set point cutoffs is a typical time diagram that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality , p. 26*
- STx: Further information see *Start and Stop Counter Functionality , p. 26*

4.4 Repetitive Counter

Overview

Introduction

This section describes the operating modes of EHC 105 if it is working as a repetitive counter.

What's in this Section?

This Section contains the following Maps:

Operating Mode 5

Characterization

The repetitive counter is an up / down counter with up to two output set points, a fast final set point, which acts as a third set point and a timed final set point.
As a repetitive counter, every time the final set point value is reached, the following restrictions apply:

- E/Sx values are limited to the value ranges 0...(2 exp 16) -1.
- The final set point value cannot be changed when the counter is active. BEA must be set in advance.
- The final set point value must be equal or greather than 2.

Operating Mode

The repetitive counter has the following operating mode:

Operating Mode	Description
5	With serial output activation.

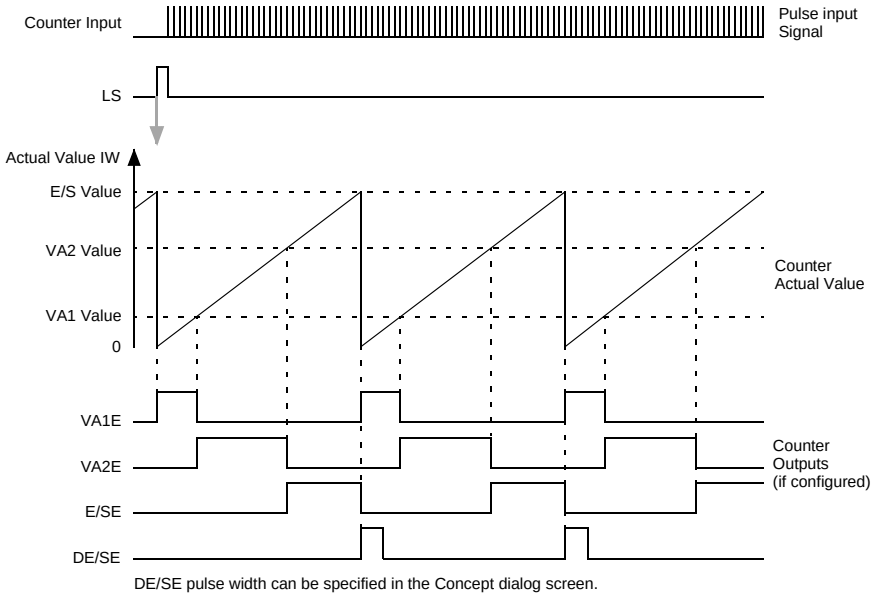
Synchronisation

This enable / disable counter input is usable for synchronisation with an external event.
The next counting pulse after an edge 0->1 at the enable / disable counter input is setting the actual value to 0 or to final setpoint value, dependent from up or down counting mode.

Time Diagram for Operating Mode 5

Counting up

Counting up is realised with VRx = 0.



DE/SE pulse width can be specified in the Concept dialog screen.

Further Signals

DE/SE pulse width can be specified in the Concept dialog screen.
This repetetive counter is a typical time diagram that do not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality , p. 26*
- STx has no effect in this operating mode.

4.5 Rate Counter

Overview

Introduction

This section describes the operating modes of EHC 105 if it is working as a rate counter.

What's in this Section?

This Section contains the following Maps:

Operating Modes

Characterization

The rate counter counts the number of pulses per unit time. A unit time is specified with the choice of the operating modes 6 or 7. The read value is then saved as the actual value.
The determined actual value thus represents the pulse count per unit time, and can be used to determine velocities, flow rates, or even revolutions.
Inputs and outputs are not processed in this counter type.
The watchdog timer function is not supported.

Operating Mode

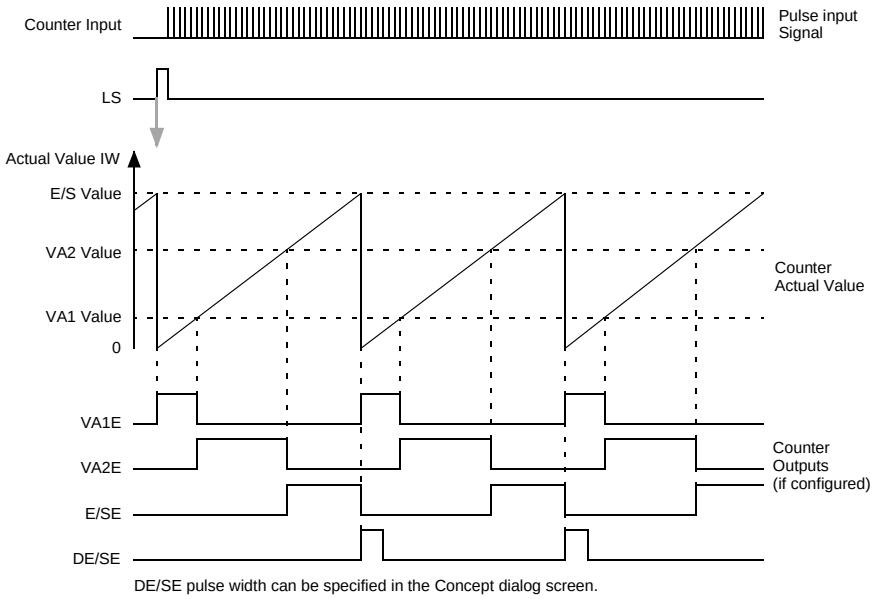
The rate counter has the following operating mode:

Operating Mode	Description
6	The gate time t amounts to 100 ms.
7	The gate time t amounts to 1 ms.

Time Diagram for Operating Modes 6 and 7

Counting up

Counting up is realised with VRx = 0.



DE/SE pulse width can be specified in the Concept dialog screen.

Further Signals

DE/SE pulse width can be specified in the Concept dialog screen.
This repetetive counter is a typical time diagram that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality , p. 26*
- STx has no effect in this operating mode.

State RAM I/O Structure

5

At a Glance

Introduction

This part includes information about the assignment between counter signals and state RAM references (3x... and 4x...).

What's in this Chapter?

This Chapter contains the following Maps:

Assignment of Input Structure

Assignment

State RAM input structure (EHC 105 00 -> CPU), word addressing:

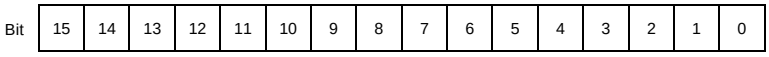
3x Registers	Relative Address	Content	
3x	000		Input status word 1
3x+1	001		Input status word 2
3x+2	002	Low word	Counter 1
3x+3		High word	Actual value
3x+4	004	Low word	Counter 2
3x+5		High word	Actual value
3x+6	006	Low word	Counter 3
3x+7		High word	Actual value
3x+8	008	Low word	Counter 4
3x+9		High Word	Actual value
3x+10	010	Low word	Counter 5
3x+11		High word	Actual value

Note: Notice the following:
- Quantum local drop: The relative address relates to the Concept configuration **In Ref** address, refer to *Configuration Steps, p. 90*.
- In Concept, the actual counter values are shown as decimal values (signed 32bit).

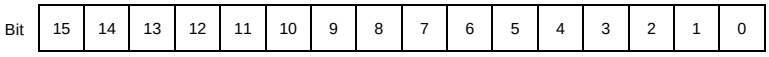
Input Status Word

Input status word 1 and 2 and their signal names:

Input Status Word 1
3x



Input Status Word 2
3x+1



	Input Status Word 1: 3x + 0	**Input Status Word 2: 3x+1**
Bit address	**Signal name**	**Signal name**
15 (MSB)	--	--
14	--	--
13	--	--
12	E/SE5	VA2E5
11	E/SE4	VA2E4
10	E/SE3	VA2E3
9	E/SE2	VA2E2
8	E/SE1	VA2E1
7	US24	--
6	SC	--
5	INDICATE	--
4	ERR5	VA1E5
3	ERR4	VA1E4
2	ERR3	VA1E3
1	ERR2	VA1E2
0 (LSB)	ERR1	VA1E1
MSB = most significant bit; LSB = least significant bit		

Input Signal Explanations

Input status word signal explanations:

Signal	Value	Meaning
Input Status Word 1		
ERRx	1	Error in counter x (specified by indicate; thus bit 5 in status word 1)
INDICATE	0	Counter overflow (actual value > 2 exp (31)-1)
1		Counting pulse error (counter timeout value expired)
SC	1	Discrete output short circuit or overload
US24	1	External power failure (discrete outputs)
E/SEx	1	Final set point signal on counter x is 1 signal
Input Status Word 2		
VA1Ex	1	First set point signal on counter x is a 1 signal
VA2Ex	1	Second set point signal on counter x is a 1 signal

Note: Output inversions (E/SEx, VA1Ex, VA2Ex) are not used on the corresponding bits in status words 1 and 2.

Assignment of Output Structure

Assignment

State RAM ouput structure (CPU -> EHC 105 00), word addressing:

4x Register	Relative Address	Content		
4x	000		Output control word 1	
4x+1	001		Output control word 2	
4x+2	002		Output control word 3	
			Counter 1	
4x+3	003	Low word	Stop value	for VR1 = 0, final set point value E/S1
4x+4		High word	Initial value	for VR1 = 1, final set point value E/S1
			Counter 2	
4x+5	005	Low word	Stop value	for VR2 = 0, final set point value E/S2
4x+6		High word	Initial value	for VR2 = 1, final set point value E/S2
			Counter 3	
4x+7	007	Low word	Stop value	for VR3 = 0, final set point value E/S3
4x+8		High word	Initial value	for VR3 = 1, final set point value E/S3

4x Register	Relative Address	Content		
			Counter 4	
4x+9	009	Low word	Stop value	for VR4 = 0, final set point value E/S4
4x+10		High word	Initial value	for VR4 = 1, final set point value E/S4
			Counter 5	
4x+11	011	Low word	Stop value	for VR5 = 0, final set point value E/S5
4x+12		High word	Initial value	for VR5 = 1, final set point value E/S5

Note: Quantum local drop: The relative address relates to the Concept configuration **Out Ref** address, refer to *Configuration Steps, p. 90*.

Output Control Word

Output control words 1, 2 and 3 and their signal names:

Output Control Word 1
4x

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB															LSB

Output Control Word 2
4x+1

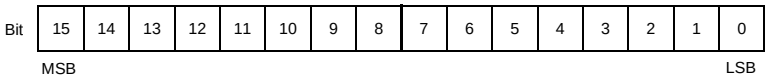
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB															LSB

Output Control Word 3
4x+2

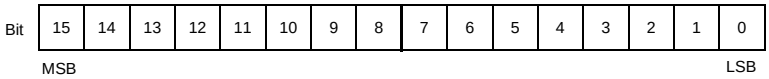
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB															LSB

	Output control word 1: 4x + 0	**Output control word 2: 4x+1**	**Output control word 3: 4x+2**
Bit address	**Signal name**	**Signal name**	**Signal name**
15 (MSB)	Counter 1 operating mode See following table	Counter 3 operating mode See following table	Counter 5 operating mode See following table
14			
13			
12			

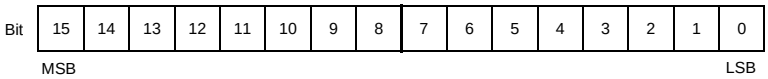
Output Control Word 1
4x



Output Control Word 2
4x+1



Output Control Word 3
4x+2



	Output control word 1: 4x + 0	**Output control word 2: 4x+1**	**Output control word 3: 4x+2**
Bit address	**Signal name**	**Signal name**	**Signal name**
11	VR1	VR3	VR5
10	BEA1	BEA3	BEA5
9	ST1	ST3	ST5
8	LS1	LS3	LS5
7		Counter 2 operating mode See following table	Counter 4 operating mode See following table
6			
5	EBUA		
4	VAR		
3		VR2	VR4
2		BEA2	BEA4
1	FQ	ST2	ST4
0 (LSB)	Q	LS2	LS4
MSB = most significant bit; LSB = least significant bit			

Output Signal Explanations

Output control word signal explanations:

Signal	Value (hex)	Meaning
Counter x operating mode	1	Event counter with parallel set point activations.
	2	Event counter with serial set point activations.
	3	Differential counter with parallel set point activations (only applies to counters 1 and 3, the set points and actual values of counters 2 respectively 4 are inactive).
	4	Differential counter with serial set point activations (only applies to counters 1 and 3, the set point and actual values of counters 2 respectively 4 are inactive).
	5	Repetitive counter
	6	Rate counter, gate time t = 100 ms
	7	Rate counter, gate time t = 1 s
	8	Event counter with parallel set point activations and fast final set point.
	9	Event counter with serial set point activations and fast final set point.
	A (default)	Event counter with timed "on" outputs, the pulse width setting holds for all employed outputs.
	B	Event counter with latched set point outputs.
	0, C, D, E, F	As operating modes A.
VRx	0	Counter x counts up
	1	Counter x counts down
BEAx	1	Counter x Output switch-off
STx	1	Counter x restart (controlled by rising edge)
LSx	1	Counter x load/start (controlled by rising edge)
EBUA	1	Outputs retain their current state on communication errors.
	0	Outputs go to 0 signal on communication errors.
VAR	1	Output set points (values) are relative for all counters.
	0	Output set points (values) are absolute for all counters.
Q	1	Acknowledgement for all counter channels after an output short circuit fault signal (SC). The red LED (F) extinguishes.
FQ	1	Acknowledgement after counter errors (ERR1...ERR5 and Indicate). The red LED (F) extinguishes. If several errors are present, they must be acknowledged individually one after the other. Counter overflow only can be acknowledged after LS was active.

	**CAUTION**
	Risk of brusque operating changes If the counter's operating mode, counting direction, switchoff behaviour or type of set point are changed while the output signals are active, the output will be deactivated and the new changes will take effect. **Failure to observe this precaution can result in injury or equipment damage.**

Monitoring and Start-Up

6

At a Glance

Introduction

This chapter includes information about monitoring and start up of the EHC 105 00 module.

What's in this Chapter?

This Chapter contains the following Maps:

Monitoring Incoming Pulses

Input Monitoring Function

The EHC 105 00 can monitor the presence or absence of incoming pulses.
If a pulse is not detected at the respective input of a running counter within the declared timeout interval, then the transmitter error flag (**indicate**) is changed to 1 and the corresponding error bit (**ERR**) is on, triggering a forced output switchoff and F-LED is on.

Note: In operating modes 6 and 7 count pulse monitoring is not supported. Refer to *Operating Modes, p. 48*.

Monitoring Requirements

To activate signal monitoring, it is necessary to state a value between 1 and 255 in the Concept dialog screen for **Counter Watchdog Time**. This fixes the counter's watchdog timers within the limits from 100 ms to 25.5 s.
Counting pulse monitoring for the respective counter occurs when the counting pulse is enabled and the counter is running. The prerequisite is the specification of a watchdog time.

Note: No monitoring is performed for 0 values.

Overflow Notification

Overflow notification:

Mode	Description
Up counting	The counter overflow is detected at an actual value of > 2 exp (31)1.
Down counting	The counter overflow is detected at an actual value of > 2exp (31).

Note: For further information see *EHC 105 00 High Speed Counter Modul Description, p. 73*.

Quantum System Bus Monitoring

Monitoring Function

A "system active" signal is activated on the Quantum system bus. If the CPU fails, all outputs are set accordingly and the green ACTIVE status LED turns off.

Output Behavior

The status of the outputs in the event of a communication failure between the controller and the EHC 105 00 can be selected through the EBUA output register bit (4x...).

Signal	Meaning
1	The current output state is retained.
0	All employed outputs are set to 0 level.

US24 Monitoring

Monitoring Function

Monitoring Function:

If...	Then ...
the external 24VDC power supply fails during operation,	● the green P-LED turns off and is shown in the module status byte, ● and the red F-LED turns on.
the power returns,	● the P-LED turns on, ● and the F-LED turns off.

Output Behavior

The discrete output (OUT1...OUT8) status displays (1 to 8) turn off; independent of the defined output logic (positive or negative).
An output switchoff is not triggered for a running counter.

Start-Up Characteristics

What Happens at Start-Up

At EHC 105 00 startup the following happens:

Stage	Description
1	All actual values are cleared to 0.
2	Outputs are deactivated (that is VA1E = VA2E = E/SE = 0).
3	The counters are defaulted to: ● upevent counters, ● absolute output set point values (VAR = 0) and ● outputs in operating mode A (timed control mode).
4	Outputs are set to 0 (EBUA = 0) on controller communications failure with the EHC105.
5	By default, all counters are enabled.

Assignments for Discrete I/O

Start-up assignment for discrete I/O

Counter Input/Output	Discrete Signal	Pin Assignments
Counter 1		
LS1 (Load and Start)	IN1	21
ST1 (Restart)	IN1	21
BEA1 (Output switch-off)	IN6	26
Counting Pulse 1	5C1/24C1	1/11
VA2E1	OUT6	36
E/SE1	OUT1	31
Counter 2		
LS2 (Load and Start)	IN2	22
ST2 (Restart)	IN2	22
Counting Pulse 2	5C2/24C2	3/13
E/SE2	OUT2	32
Counter 3		
LS3 (Load and Start)	IN3	23
ST3 (Restart)	IN3	23
BEA3	IN7	27
Counting Pulse 3	5C3/24C3	5/15
VA2E3	OUT7	37
E/SE3	OUT3	33
Counter 4		
LS4 (Load and Start)	IN4	24
ST4 (Restart)	IN4	24
Counting Pulse 4	5C4/24C4	7/17
E/SE4	OUT4	34
Counter 5		
LS5 (Load and Start)	IN5	25
ST5 (Restart)	IN5	25
Counting Pulse 5	5C5/24C5	9/19
BEA5	IN8	28
VA2E5	OUT8	38
E/SE5	OUT5	35

EHC 105 00 High Speed Counter Modul Description

II

At a Glance

Introduction

This part includes the module description about the High Speed Counter EHC 105 00.

What's in this part?

This Part contains the following Chapters:

EHC 105 00 High Speed Counter Modul Description

7

At a Glance

Introduction

This chapter includes information about the module description for EHC 105.

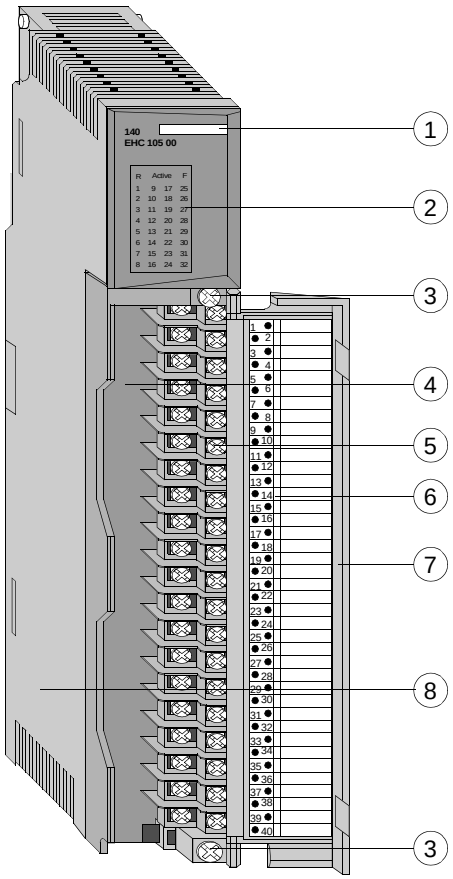
What's in this Chapter?

This Chapter contains the following Maps:

EHC 105 00 Hardware Overview

User accessable Parts

EHC 105 00 module front view



1 Color Code

2 LED Status Display

3 I/O Block Mounting Screws

4 I/O Block

5 Terminal Block

6 Label Inlay (Inner Side)

7 I/O Block Cover

8 Standard-Size Module (Housing)

HW Overview

The EHC 105 00 module is a highspeed counter with the following features:

- Counted value processing for five pulse generators (counter inputs isolated from one another):
  - 5 VDC, fmax = 100 kHz for cable lengths of up to 100 m
  - 24 VDC, fmax = 20 kHz for cable lengths of up to 100 m
- 8 isolated inputs and outputs with LED status display
- Short circuitproof output
- Backplane provides the internal 5 VDC supply
- Configuration assignment is made by the CPU

Functionality Overview

Five equivalent, independently usable counters with the following functions are utilized:

- 32bit event counter with 6 modes
  - Event counter with parallel set point output activation
  - Event counter with parallel set point output activation and fast Final Set Point
  - Event counter with serial set point activation
  - Event counter with serial set point activation and fast final set point
  - Event counter with timed set point output activation
  - Event counter with latched set point output avtivation
- 32bit differential counter (2 configurable counter pairs) with 2 modes
  - Differential counter with serial set point output activation
  - Differential counter with parallel set point output activation
- 16bit repetitive counter
- 32bit (velocity counter, rate counter) with 2 modes
  - Rate counter with 100ms gate time
  - Rate counter with 1s gate time

Note: For the operating mode assignments to their mode identifiers, refer to *Mode Number of Counter Types, p. 39*.

EHC 105 00 Hardware Specifics

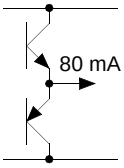
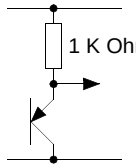
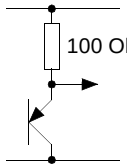
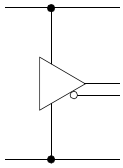
Cable Specifics

The cable specifics are as follows:

- Shielded, twisted pair cable is to be utilized for pulse generator connection to the counter inputs.
  - JELiYCY 2 X 2 X 0.5 (Order no.: 424 234 035)
  - JELiYCY 5 X 2 X 0.5 (Order no.: 424 238 059)
- The shield should have a short connection (< 20 cm) with ground at one cable end.
- Be sure not to install the cabling together with power lines or other similar sources of electrical disturbance. Clearance > 0.5 m.
- Input connecting cables, bulk:
  - JELiYCY 2 X 2 X 0.5 twisted pair, (Order no.: 424 234 035).
  - JELiYCY 5 X 2 X 0.5 twisted pair, (Order no.: 424 238 059).

Note: Pay attention to cable length dependencies upon transmitter frequencies and output type.

Maximum Cut-Off Frequencies

Transmitter Output	Circuit Diagram	Transmitter Output Level(VDC)	Cable Length (m)	Max. Transmitter Frequence (KHz)
Push-Pull Driver	Push-pull (24) 	24 24 24	30 100 300	35 20 10
NPN Driver (open collector)	NPN (24) 	24 24 24	30 100 300	35 20 10
NPN Driver (open collector)	NPN (5) 	5 5	30 300	100 100
SN 75 178 line driver	SN 75 178 (5) 	5 5	30 300	100 100

EHC 105 00 Hardware Configuration

Voltage Supply

The EHC 105 00 module is supplied by the Quantum bus with VCC = 5 VDC. The isolated I/O and the counter inputs are an exception. They receive the working voltage US24 = 24 VDC provided by an external power supply. The green P-LED lights when US24 is present.
In addition, if the 24 VDC is not present, status bit 7 is set and the FLED turns on. If the 24 VDC is present again, status bit 7 is reset and the FLED turns off.

Note: The alternatively available 5 VDC counter inputs may also be used.

Hot Swap

As for all Quantum modules, you can remove and insert the module during bus operation. However, module reconfiguration is required.

Counter Inputs

The counter inputs are isolated from one another and from the discrete I/O. Each counter input is present in two variations, whereby 5C1...5C5 are for 5 VDC signals and 24C1...24C5 for 24 VDC signals.
All input signals are displayed by green LEDs. (Refer to *LED Status Display, p. 80*).

WARNING

Risk of hardware configuration failure

Only transmitters with 5 VDC output signals may be connected to 5C1...5C5. From each counter input only one connection (either 5 VDC or 24 VDC) may be utilized.

Failure to observe this precaution can result in severe injury or equipment damage.

Counter Input Example

There is exactly one reference potential per counter input (M11...M15):
- 5 VDC transmitter on counter 4: using terminals 5C4 and M14
- 24 VDC transmitter on counter 4: using terminals 24C4 and M14

Conter Enable

To every counter a hardwarerelated input (IN1...IN5) is assigned as counter enable (gate function). Whether the input is to be used as counter enable can be selected separately for each counter channel through the configuration dialogs of Concept. The input may be used for other functions, should it not be allocated as counter enable. The counter input is then always enabled.

Discrete Inputs

The module is equipped with five counter and eight discrete inputs, each of which can be assigned different functions.
Discrete inputs are isolated from the back plane.
All input signals are displayed by green LEDs. (Refer to *LED Status Display, p. 80*).
The discrete inputs can be assigned the following functions:

- Counter enable (gate function)
- Counter load/start (outputs set)
- Counter restart (outputs set)
- Output switchoff trigger (resets outputs VA1Ex, VA2Ex and E/SEx)
- Input signal states can be inverted

Note: Notice following:

- The load/start respectively restart functions are combined by a logical AND with the LSx respectively STx state RAM bits.
- If no hardware input is utilized for load/store respectively restart, then the AND condition is met, if the bit in state RAM is set.
- In the event counter modes (operating modes 1 and 2) and differential counter mode (operating modes 3 and 4), the restart command is only possible after an output switchoff (BEAx).
- The restart command is not possible in the repetitive counter (mode 5), velocity counter (modes 6 and 7), and event counter with fast output switchoff (modes 8 and 9) operating modes.
- The functions can be chosen in the Concept I/O mapping list with the **Params** button.

Discrete Outputs

The module has eight discrete outputs. All outputs are short circuit proof and overloadproof (Imax = 500 mA), and have potential isolation with respect to the inputs and back plane (I/O bus).
To the outputs the following functions can be assigned:

- First set point (timed for mode A)
- Second set point (timed for mode A)
- Final set point (timed for mode A)
  Module outputs assigned to the final set point of those operating modes making use of the fast final set point are processed particularly fast:
  - without fast final set point: typically 3 ms
  - with fast final set point: typically 0.5 ms
- Timed final set point (with choice of pulse width)
- Output signal states can be inverted

Note: The functions can be chosen in the Concept I/O mapping list with the **Params** button.

Short Circuit

Short circuit of one or more outputs leads to a fault message (the red F-LED lights). As soon as the short circuit has been neutralized, the outputs can be returned to normal operation per collective reset signal Q.

Power-Up

At powerup (back plane 5 VDC) all discrete outputs are inactive. On master station failure all outputs are deactivated. (The outputs go to 0 with positive logic and 1 with negative logic).

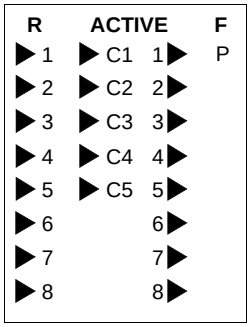
Jumpers

The module is delivered without jumpers. The module's contact strips are only used for test purposes.

LED Status Display

Status Display Front View

LED status display front view (LED numbering):



Explanation of the LED status display:

LED	Color	Description
R	green	READY - module is ready (firmware initialization has been completed).
P	green	POWER - the US24 working voltage is present.
ACTIVE	green	The PLC communication becomes active.
1 to 8	green	Display the signal states of the discrete inputs IN1...IN8.
1 to 8	green	Display the signal states of the discrete outputs OUT1...OUT8.
C1 to C5	green	Light with the clock frequency applied to clock-inputs 5C1 respectively 24C1 to 5C5 respectively 24C5.

Fault Display

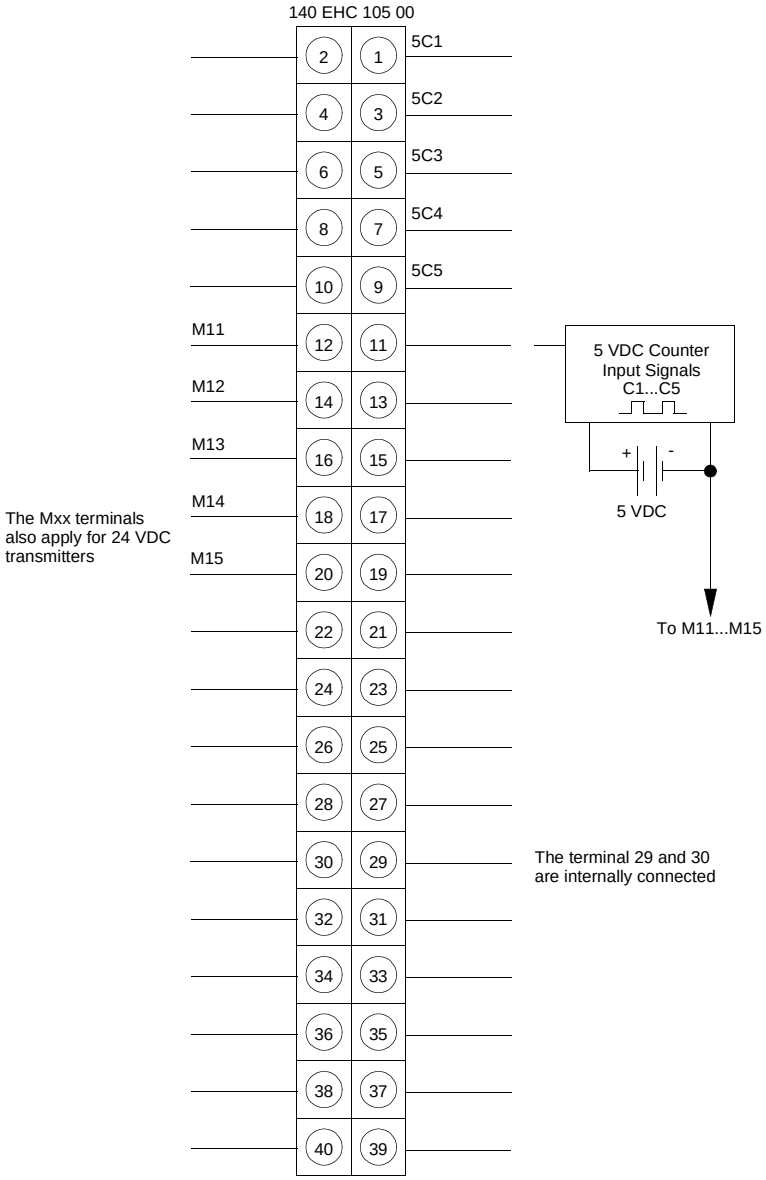
The red F-LED (F = fault) lights on the following faults:

- 24 VDC supply voltage (US24) not present
- Short circuit on one of the OUTn outputs
- Pulse monitoring has tripped (indicate bit = 1 and ERRx = 1)
- Counter overflow (indicate bit = 0 and ERRx = 1)

EHC 105 00 Hardware Wiring

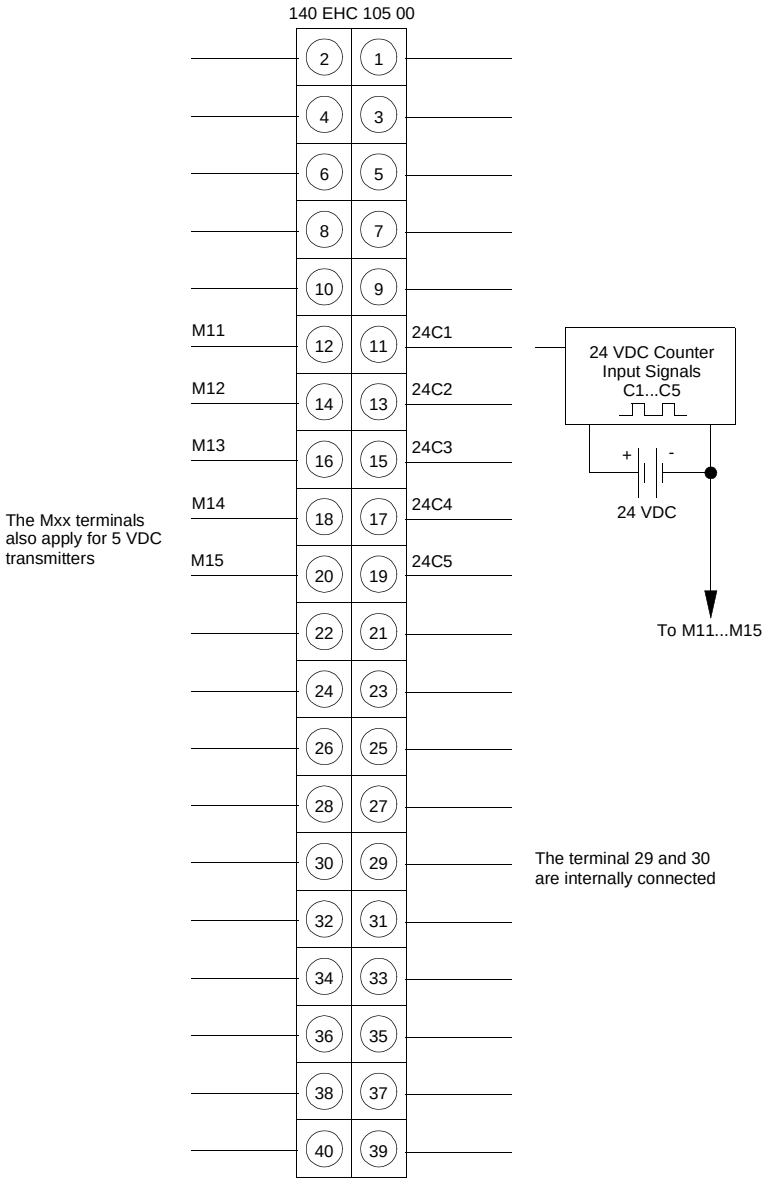
5Cx Counter Inputs

Wiring diagram for 5Cx counter inputs.



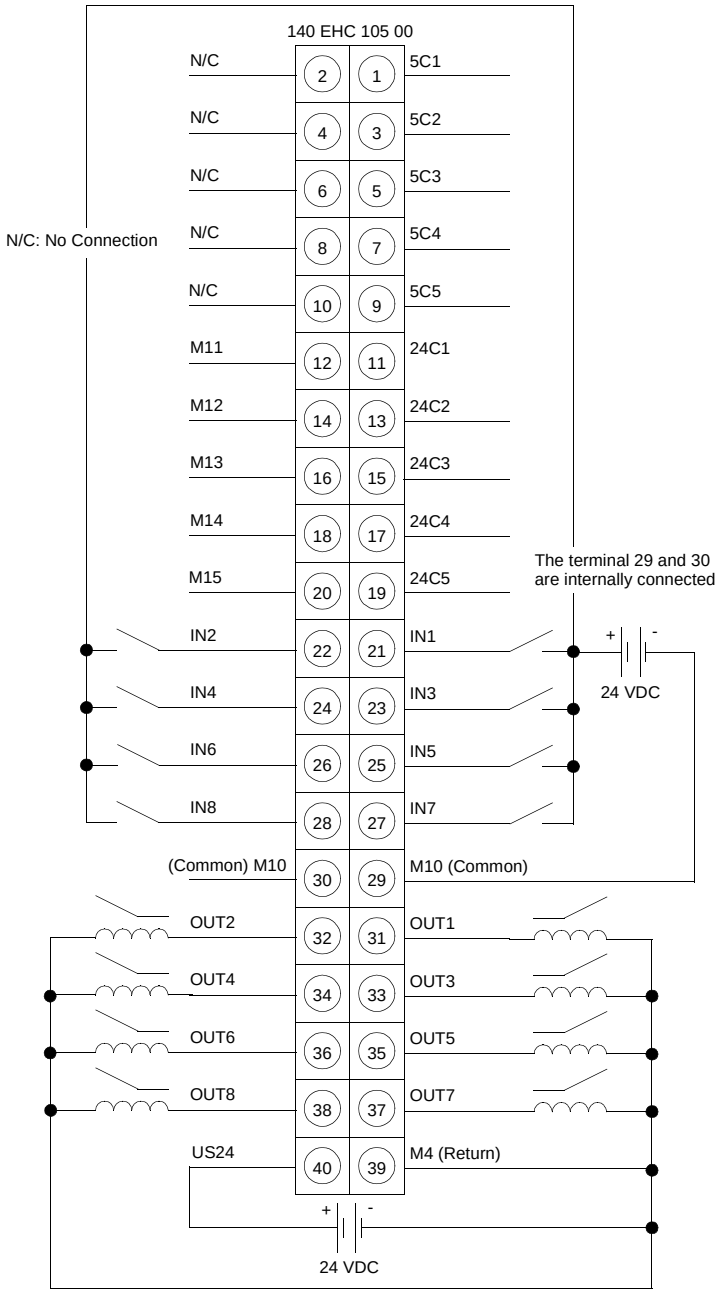
24Cx Counter Inputs

Wiring diagram for 24Cx counter inputs.



Discrete Inputs and Outputs

Wiring diagram for discrete inputs and outputs.



EHC 105 00 Hardware Technical Specifications

General

General technical specifications are as follows:

- 5 counter inputs
- 8 discrete inputs
- 8 digital outputs
- 12 words IN
- 13 words OUT

LED display:

LED	Color	Description
ACTIVE	-	-
F	-	-
R	green	Modul is ready
1 ... 8 (left)	green	Discrete inputs (IN1 ... IN8)
C1 ... C5	green	Counter inputs (C1 ... C5)
1 ... 8 (right)	green	Discrete outputs (OUT1 ... OUT8)
P	green	Power on

Counter Inputs

Counter input specifications

Counter Inputs	5V	24V
Count frequency (100KHz)	@5 VDC, further information see *EHC 105 00 Hardware Specifics, p. 76*.	--
Count frequency (20KHz)	@5 VDC, further information see *EHC 105 00 Hardware Specifics, p. 76*.	@24 VDC, further information see *EHC 105 00 Hardware Specifics, p. 76*
Count to output assertion delay (Max)	3ms	3ms
Input voltage	OFF state (VDC) :1,0 ... +1,15 ON state (VDC): 3,1 ... 5,5	OFF state (VDC): -3,0 ... +5,0 ON state (VDC):15,0 ... 30,0
Input current	8 mA for 3,1VDC	7 mA for 24 VDC
Duty cycle	1 : 1	1 : 1
Data formats	16 bit counter: 65.535 Decimal 32 bit counter: 2.147.483.647 Decimal	16 bit counter: 65.535 decimal 32 bit counter: 2.147.483.647 decimal
Delay time (typical)	t = 0,002 ms	t = 0,002 ms

Discrete Inputs

Discrete input specifications 24 VDC

Discrete Inputs	**24V**
VREF supply +24VDC	Off State (VDC): -3,0 ... +5,0 ON State (VDC):15,0 ... 30,0
Delay time (typical) IN1 ... IN6 IN7, IN8	 ton = 2,2 ms, toff = 1 ms ton = 0,006 ms, toff = 0,3 ms
Input current (typical)	5 mA

Discrete Outputs

Discrete output specifications

Discrete Outputs	**24V**
Switch ON	20 ... 30 VDC
Switch OFF	0 VDC (ground reference)
Max load current (each output)	0,5 A
Output off state Leackage	0,1 mA max @ 30 VDC
Output on state voltage drop	1,5 VDC @ 0,5 A

Miscellaneous

Different specifications

Miscellaneous	
Isolation (channel to bus)	500 VAC rms for 1 minute
Fault detection	Loss of output field power, output short circuit
Power dissipation	Maximum 6W
Bus current required	250 mA
External 24 VDC power supply	19,2 ... 30 VDC, 24 VDC nominal, 60 mA reqired plus the load current for each output.
External fusing	User discretion
Compatibility	Programming software and Quantum controllers: see *Hardware and Software Prerequisites, p. 90*.

Note: The 5Cx and 24Cx counter inputs may be used alternatively.

Configuration using Concept

III

At a Glance

Introduction

This part includes information about the configuration of EHC 105 00 with examples.

What's in this part?

This Part contains the following Chapters:

Prerequisites, Drop and Counter Characteristics Configuration

8

At a Glance

Introduction

This part includes information about start of installation and configuration of different counter types with examples.

What's in this Chapter?

This Chapter contains the following Maps:

Hardware and Software Prerequisites

Prerequisites

Hardware and software prerequisites are as follows:

- PC for Concept
- Software package: Concept Version 2.0
- CPU EXEC Version 2.0
- Quantum System with any CPU refer to the Quantum Reference Guide (840 USE 100 00)

Note: Notice the following:

- This module is also supported with Concept 1.13, but version 2.0 or greater is recommended.
- The screens, described in this document are made with version 2.0 or higher.

Configuration Steps

Introduction

The steps necessary for configuration are presented here. Where additional information is necessary, references to the corresponding documentation is made.

Steps for Configuration

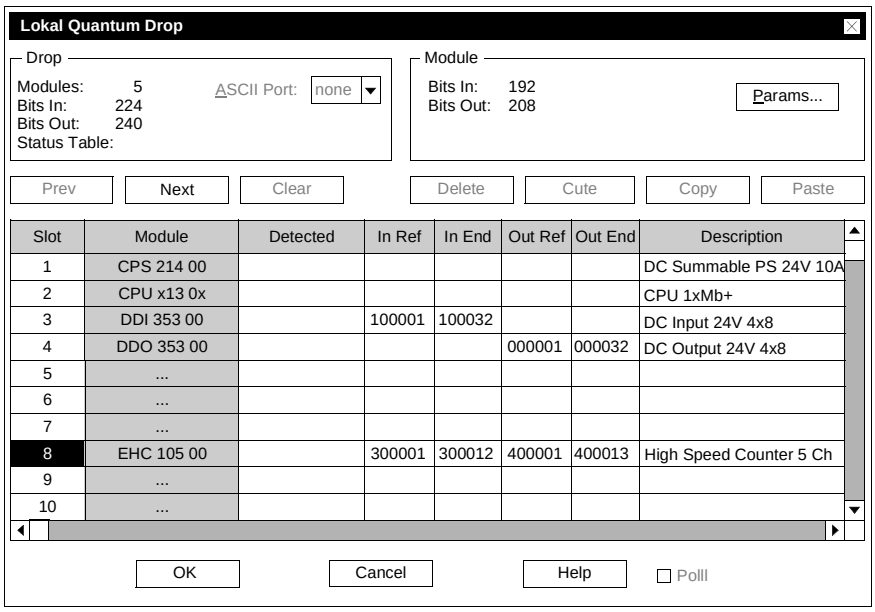
Following steps are necessary:

Step	Description
1	Configure your controller in accordance with your requirements, also with respect to the EHC 105 00, as described in the Quantum Hardware Reference Guide (840 USE 100 00). Details for connecting signal transmitters to the EHC 105 00 can be found within the *EHC 105 00 High Speed Counter Modul Description, p. 73*.
2	Plan and carry out the module cabling in accordance with the module details (that is cable routing, shielding and so on).
3	Log your terminal assignment plan on the label inlay inside the module I/O block cover.

Configuration of Local Quantum Drop

Drop Configuration

Configuration using Concept (Slot and I/O Map)



Terminology

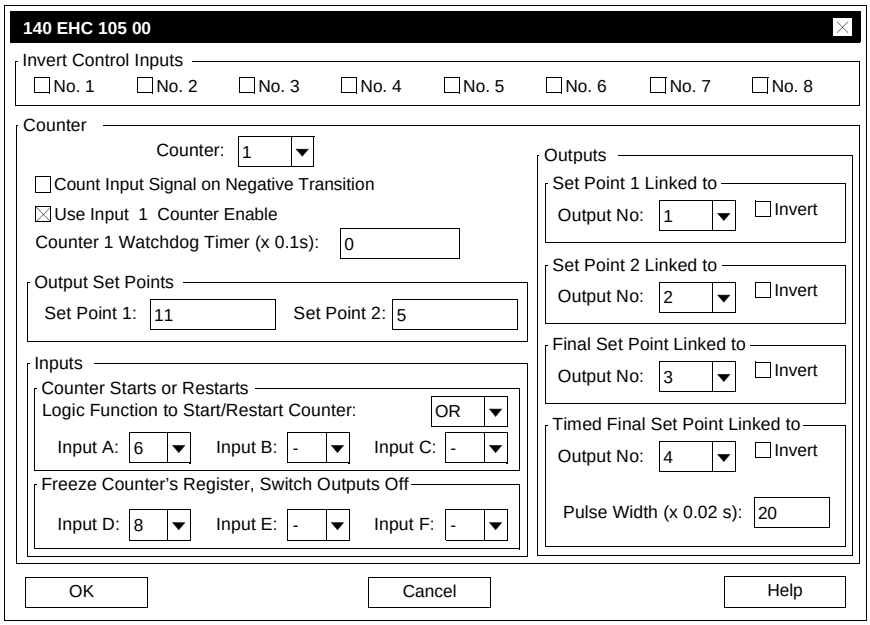
Drop editor terminology explanations:

Term	Meaning
Clear	Configuration deletion for all slot resident modules
Delete	Deletion of the selected module
Params...	Starts the configuration dialog (see following screen)
Slot	Selects the slot for module entry
Module	Starts the module configuration dialog
Detected	Modules recognized on-line
In Ref	State RAM initial address (for input)
In End	State RAM calculated end address (for input)
Out Ref	State RAM initial address (for output)
Out End	State RAM calculated end address (for output)
Description	Short module description
OK	Accepts all inputs

Configuration of Counter Characteristics and I/O Map

Characteristics Configuration

For Counter 1 the following EHC 105 00 settings are selected with the Concept dialog screen:



Terminology

Quantum I/O map editor terminology explanations:

Term	Meaning
Invert Control Inputs	Select inversion of all discrete inputs (IN1...IN8).
Counter	Selection of the individual counters.
Count Input Signal on Negative Transition	Select inversion of the counter inputs.
Use Input No. 1 for Counter Enable	Select Input 1 to enable counter.
Counter 1 Watchdog Time (x 0.1s):	Counter Watchdog time setting in 0.1s steps, 0 disables counting pulse monitoring.
Output Set Points•.[Text:Field]2 - Relative	If relative Output Set Point mode is selected, output Set Point Values are relative to the Final Set Point Value. Requirement for that: E/S > VA1 >= VA2 >= 0.
-Absolute	If absolute Output Set Point mode is selected, this value is absolute. Requirements for that: E/S > VA2 >= VA1 >= 0.

Term	Meaning
Logic Function to Start/ Restart Counter	Logic function among inputs to Load / Start or Restart the counter.
Input A:, B:, C:	Assignment of up to 3 process inputs for load/start and restart function control.
... Switch Outputs Off	Assignment of up to 3 process inputs (D:, E:, F:) to Output Switch-Off.
Set Point 1 linked to ...	Assignment (and optional inversion) of a discrete output to the first set-point.
Set Point 2 linked to ...	Assignment (and optional inversion) of a discrete output to the second set-point.
Final Set point	Assignment (and optional inversion) of a discrete output to the final set-point.
Timed Final Set Point	Assignment (and optional inversion) of a discrete output to the timed final set-point.
Pulse Width (x 0.02s):	Setting of the Timed Final Set Point pulse width (0...255). 0 disables the output.

Classification and Assignment of Derived Data Types

Introduction

Derived data types simplify access to the EHC 105 00's input and output signals. The EHC 105 00 is mapped to word registers. The derived data type structures provided are composed of bytes and double words (WORD 32). Should you wish to have access to individual bits, the corresponding bytes must first be converted to bit strings.

Classification

The following derived data types are available for the EHC 105 00:

Derived Data Types	Valid for:	Memory Utilization
EHC105_IN	EHC 105 00 input data	12 input words
EHC105_OUT	EHC 105 00 output data	13 output words

Input Assignement

The assignment between EHC 105 00 data elements and Type and function for input data is as follows:

Element	Data Type	Function
error	BYTE	**Error flag status byte**
		Bit 0 = 1: Counter 1 error (ERR1)
		Bit 1 = 1: Counter 2 error (ERR2)
		Bit 2 = 1: Counter 3 error (ERR3)
		Bit 3 = 1: Counter 4 error (ERR4)
		Bit 4 = 1: Counter 5 error (ERR5)
		Bit 5 = 1: Clock error, Bit 5 = 0: Counter overflow
		Bit 6 = 1: Output short circuit
		Bit 7 = 1: External power failure
Final	BYTE	**Switch-off signals status byte**
		Bit 0 = 1: Counter 1 Final Set Point (E/SE1)
		Bit 1 = 1: Counter 2 Final Set Point (E/SE2)
		Bit 2 = 1: Counter 3 Final Set Point (E/SE3)
		Bit 3 = 1: Counter 4 Final Set Point (E/SE4)
		Bit 4 = 1: Counter 5 Final Set Point (E/SE5)
Set Point 1	BYTE	**Switch-off signals status byte**
		Bit 0 = 1: Counter 1 1st Set Point (VA1E1)
		Bit 1 = 1: Counter 2 1st Set Point (VA1E2)
		Bit 2 = 1: Counter 3 1st Set Point (VA1E3)
		Bit 3 = 1: Counter 4 1st Set Point (VA1E4)
		Bit 4 = 1: Counter 5 1st Set Point (VA1E5)
Set Point 2	BYTE	**Switch-off signals status byte**
		Bit 0 = 1: Counter 1 2nd Set Point (VA2E1)
		Bit 1 = 1: Counter 2 2nd Set Point (VA2E2)
		Bit 2 = 1: Counter 3 2nd Set Point (VA2E3)
		Bit 3 = 1: Counter 4 2nd Set Point (VA2E4)
		Bit 4 = 1: Counter 5 2nd Set Point (VA2E5)

Element	Data Type	Function
actual	ARRAY[1..5] OF WORD32	**Actual Values**
		1st WORD 32: Counter 1 Actual Value 1
		2nd WORD 32: Counter 2 Actual Value 2
		3rd WORD 32: Counter 3 Actual Value 3
		4th WORD 32: Counter 4 Actual Value 4
		5th WORD 32: Counter 5 Actual Value 5
Note: Further information see *State RAM I/O Structure , p. 59*.		

Output Assignment

The assignment between EHC 105 00 data elements and type and function for output data is as follows:

Element	Data Type	Function
Quit	BYTE	**Counter acknoledgement**
		Bit 0 = 1: Output short circuit acknowledgement (Q)
		Bit 1 = 1: Acknowledgement for under voltage and counter errors (FQ).
		Bit 2 = Don't care.
		Bit 3 = Don't care.
		Bit 4 = 1: Setpoint cutoff in relative mode, otherwise absolute (VAR).
		Bit 5 = 1: All output states retained on failure (EBUA).
		Bit 6 = Don't care.
		Bit 7 = Don't care.
Control	Array[1...5] of Byte	**Counter characteristics**
		BYTE 1 to 5: Control bytes counters 1... 5
		Bit 0 = 1: Load/start (LSx)
		Bit 1 = 1: Restart (STx)
		Bit 2 = 1: Output switchoff (BEAx)
		Bit 3 = 0: Upcounter, Bit 3 = 1: Downcounter (VRx
		Bits 4..7: Counter operation mode

Element	Data Type	Function
Final	Array[1...5] of Word32	**Final Set Point Value**
		1st Word32: Counter 1 Final Set Point (E/S1)
		2nd Word32: Counter 2 Final Set Point (E/S2)
		3rd Word32: Counter 3 Final Set Point (E/S3)
		4th Word32: Counter 4 Final Set Point (E/S4)
		5th Word32: Counter 5 Final Set Point (E/S5)

Configuration Example 1 with Event Counter (Relative)

9

At a Glance

Introduction

The following configuration example is valid for the following counter:

- Event counter, counting up
- Parallel output activation
- Counter 1 in mode 1

What's in this Chapter?

This Chapter contains the following Maps:

Configuration Order for Example Event Counter (Relative)

Configuration Order

The order of configurations is as follow:

1. Specifications
2. Hardware setup
3. Block Diagram for counter
4. Software settings using Concept
5. Start counter
6. Time diagram

Example Specifications for an Event Counter (Relative)

Output Specifications

This application describes using the counter as an event counter 1 in operating mode 1, counting up to 30 counts.
See the following specification for counter 1:

Setpoint (SP)	Linked Outputs	Active Level	Values
FSP (E/SE1)	03	1 -> 0	30 counts (E/S1)
1SP (VA1E1)	01	1 -> 0	11 counts (VA11)
2SP VA2E1)	02	1 -> 0	5 counts (VA21)
TFSP (DE/SE1)	04	0 -> 1 (400 ms)	

Note: The values for set points are relative mode.

Input / Other Specifications

Further specifications:

- Input pulse is 24 V, not inverted.
- A field signal is connected to input 8 and forces output switchoff.
- Input 1 is selected to enable the counter.
- The OR logic for the inputs sets the counter.
- Watchdog timer is shut off.
- IN6 is used to load / start, restart counter.
- If communication is lost, the counter outputs will be set to 0.

Example Hardware Set up for an Event Counter (Relative)

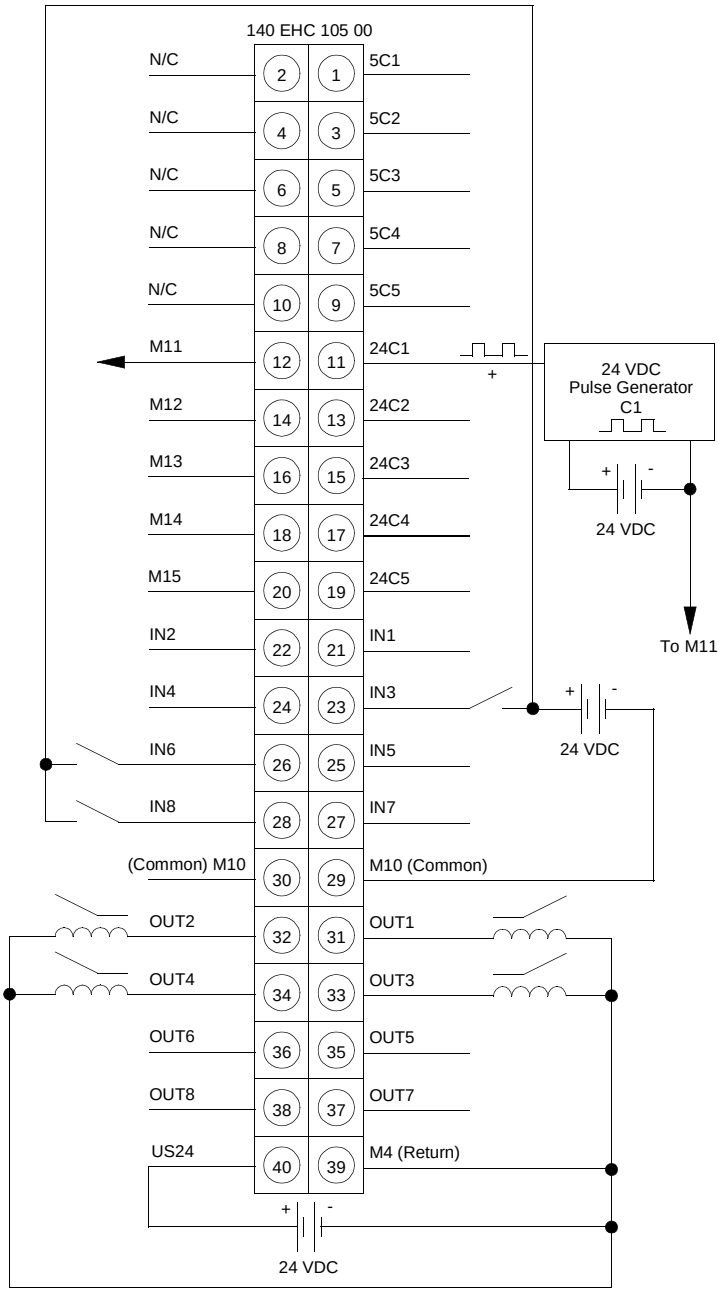
Installation Procedure

For installation follow the steps:

Step	Action
1	Install the EHC 105 00 module into the local backplane's slot 8 and secure it.
2	Install the module terminal strip.
3	Connect an external 24 VDC supply voltage (+ pin 40/ pin 39).
4	Connect the Pulse input signal to pin 11 (24VDC).
5	Complete the module wiring (see next figure).

Wiring

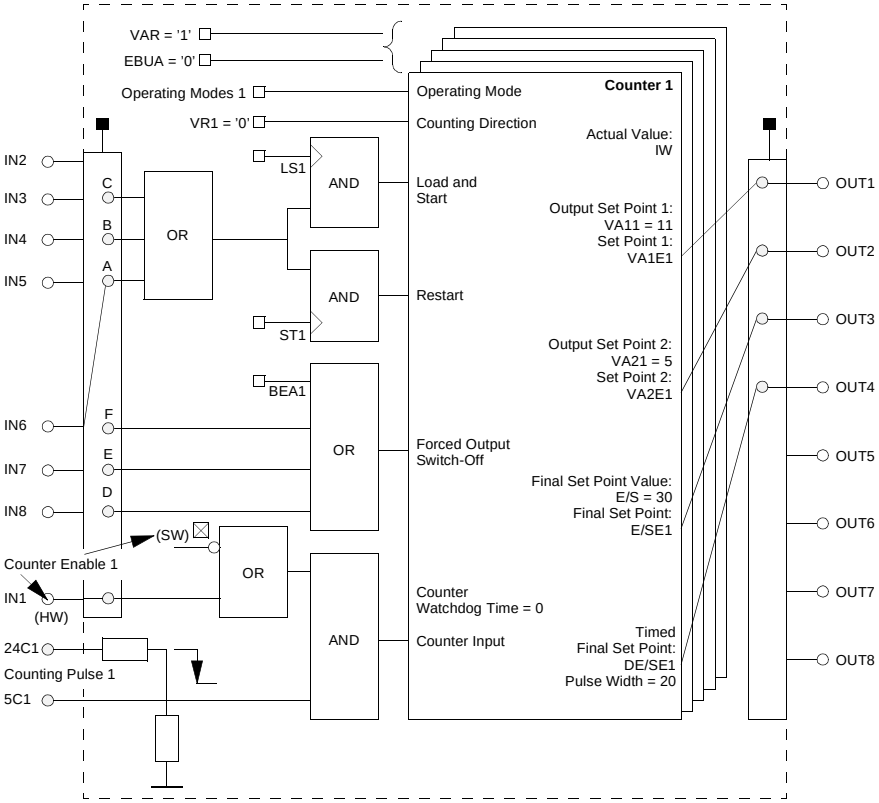
Wiring for Event Counter:



Example Block Diagram for an Event Counter (Relative)

Block Diagram

Block Diagram for event counter with parallel set point output activation at mode 1.

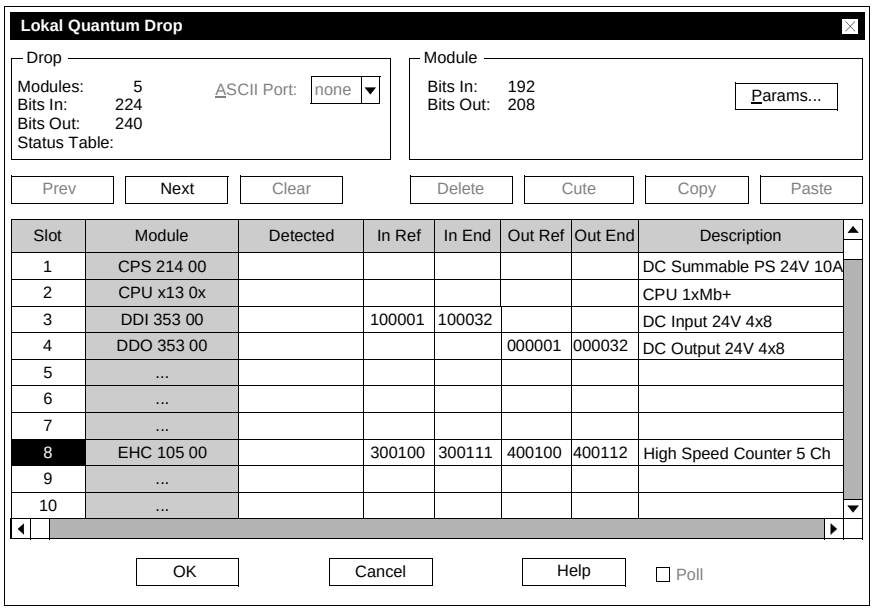


	CAUTION
	Risk of configuration failure Do not use outputs OUT1...OUT4 with other counters; such multiple usage is prohibited. **Failure to observe this precaution can result in injury or equipment damage.**

Example Software Settings Using Concept for an Event Counter (Relative)

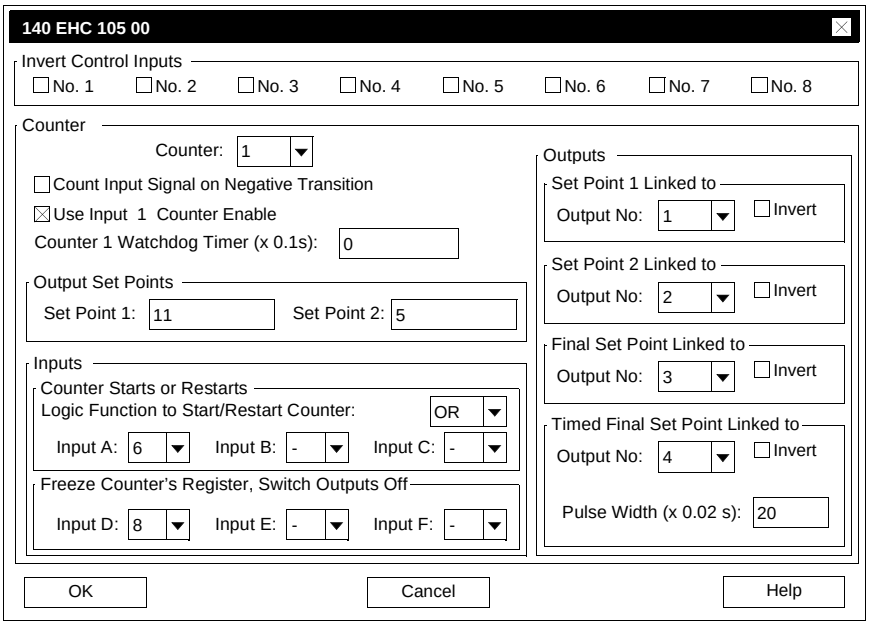
Drop Configuration

Configuration of module into slot 8 and I/O-Map:



Slot	Module	Detected	In Ref	In End	Out Ref	Out End	Description
1	CPS 214 00						DC Summable PS 24V 10A
2	CPU x13 0x						CPU 1xMb+
3	DDI 353 00		100001	100032			DC Input 24V 4x8
4	DDO 353 00				000001	000032	DC Output 24V 4x8
5	...						
6	...						
7	...						
8	EHC 105 00		300100	300111	400100	400112	High Speed Counter 5 Ch
9	...						
10	...						

I/O Configuration I/O configuration and counter 2 characteristics.



Configuration with the Help of Drop and I/O Configuration Screen for Example Event Counter (Relative)

Preconditions Stop the controller before configuring the module.

Configuration Use the following selections to configure the counter specifications within the screens above.:

Item	**Screen Selection**
Counter properties	
Counting pulse 1 with falling edge:	On Negative Transition
Counter Watchdog Time (x0,1s) = 0	Value 0 is selected
Counter enable assignment to IN1:	Input No.1 for counter enable is selected (cross).
Load/start or restart and output switchoff assignments:	
Logic Between Start Inputs: OR.	OR is selected.
Enter IN6 as load/start or restart input, no inversion.	IN6 for Input A: is selected. No cross at **Invert Control Inputs No.6**.

Item	**Screen Selection**
Enter IN8 as output switchoff, no inversion.	IN8 for Input D: is selected. No cross at **Invert Control Inputs No.8**.
Output assignments, features	
Link Set Point 1 to OUT1 , no inversion.	Out 1 is selected for Set Point 1. (Multiple usage is prohibited !!) No cross at **Invert**.
Link Set Point 2 to OUT2 , no inversion.	Out 2 is selected for Set Point 2. (Multiple usage is prohibited !!) No cross at **Invert**.
Link Final Set Point to OUT3, no inversion.	Out 3 is selected for Final Set Point. (Multiple usage is prohibited !!) No cross at **Invert**.
Link Timed Final Set Point to OUT4, no inversion.	Out 4 is selected for Timed Final Set Point. (Multiple usage is prohibited !!) No cross at **Invert**.
Timed Final Set Point Pulse Width = 400ms.	Value = 20 is entered for Pulse Width (x 0,02).
Specify Set Point Values	
Set Point 1 value: 11	Value = 11 is entered.
Set Point 2 value: 5	Value = 5 is entered.
Specify Final Set Point Value; select the 4x... register (see *I/O Configuration, p. 103*).	
Enter the Final Set Point Value (E/S1=30) as 32bit value (with user program):	**E/S1: 400103 = 30 LD** (see *Assignment of Output Structure , p. 62*).
Specify counter characteristics:	
Parallel Event Counter =0001, Counting up =0000, relative Set Point =0001 (user program)	**Register 400100 = 101**0hex (see *Assignment of Output Structure , p. 62*).

Start for Example Event Counter (Relative)

Starting the Counter

Start the controller, then follow the steps on the module data reference screen:

Step	Function	Activity	Effect

1	Load/start counter	• Activate (High) discrete Input 6 (pin 26).
		• Enter LS1 bit in 400100 register (D8 = 1 respectively 1110 hex) (with user program), (see output structure in *Assignment of Output Structure , p. 62*).
			The outputs switch to 1 signal and the counter's actual value is set to 0:
			• 300101 register:
			  • VA1E1(D0) = OUT1 = 1
			  • VA2E1(D8) = OUT2 = 1
			• 300100 register:
			  • E/SE1(D8) = OUT3 = 1
			• 300102 register:
			  • counter's actual value = 0

2	Enabling Counter 1	Activate (High) discrete Input IN1 (pin 21, counter enable).	Counter 1 counts the pulses at counter input 1: • At actual value 19 = 30-11 OUT1 switches off. • At actual value 25 = 305 OUT2 switches off. • At actual value 30 OUT3 switches off. • The Timed Final Set Point output OUT4 switches on for 400 ms.

Switch Off Out1...Out4

If the counter has not reached the final set point value, the outputs OUT1 .. OUT4 can be switched off:

- with an external 1 signal connected to input IN8 or
- through the 400100 register BEA1 bit (with D10 = 1 respectively 1410 hex, since the operating mode must be retained).

In this case all outputs and the input status word bits (300100 register (D8), 300101register (D0 and D8)) switches to 0 signal. See also *Start and Stop Time Diagram without Hardware Input Configuration, p. 27*.

Restart

Note: You can restart only after output switchoff (BEA). See also *Start and Stop Time Diagram without Hardware Input Configuration, p. 27*.

In this example a restart is possible under the following conditions:

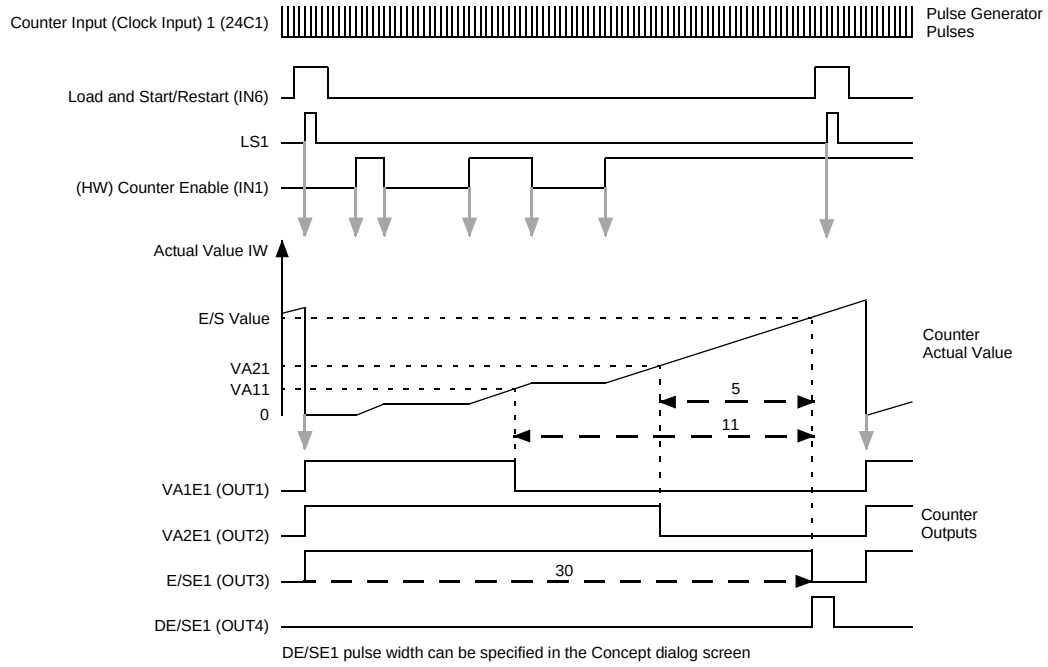
- The final set point value (example value = 30) has not been reached.
- 1 signal is activated at input IN6.
- A rising edge at the 400100 register ST1 bit (D9, respectively 1210 hex) is entered.

Load/Start When the counter is reset the counting value is set to 0 and the outputs become active again.

Example Time Diagram for an Event Counter (Relative)

Introduction When the counter is reset the counting value is set to 0 and the outputs become active again.

Time Diagram Event counter with parallel output activation (up):



Note: Notice following:

- DE/SE1 pulse width can be specified in the Concept dialog screen.
- If pulses continue to appear at counter input 1 after reaching the final set point value (30), the pulses will also be counted and displayed as the current actual value in the 300102- register as a 32-bit value.
- When the counter is reset (load/start) the counting value is set to 0 and the outputs become active again.
- If the counter's operating mode, counting direction, switch-off behavior, or type of set point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

Configuration Example 2 with Repetitive Counter

10

At a Glance

Introduction

The following configuration example is valid for the following counter:

- Repetitive counter, counting up
- Serial set point output activation
- Counter 2 in mode 5

What's in this Chapter?

This Chapter contains the following Maps:

Configuration Order for Example Repetitive Counter

Configuration Order

For this example the configuration order is as follow:

- Specifications
- Hardware setup
- Block Diagram for counter
- Software settings using Concept
- Start counter
- Time diagram

Example Specifications for a Repetitive Counter

Output Specifications

This application describes using the counter as a repetitive counter 2 in operating mode 5, counting up to 30 counts.
See the following specification for counter 2:

Setpoint (SP)	Linked Outputs	Active Level	Values
FSP (E/SE2)	03	1 -> 0	30 counts (E/S2)
1SP (VA1E2)	01	1 -> 0	11 counts (VA12)
2SP VA2E2)	02	1 -> 0	5 counts (VA22)
TFSP (DE/SE2)	04	0 -> 1 (400 ms)	

Note: The values for set points are relative mode.

Input / Other Specifications

Further specifications:

- Input pulse is 24 V, not inverted.
- A field signal is connected to input 8 and forces output switchoff.
- Input 2 is selected to enable the counter.
- The OR logic for the inputs sets the counter.
- Watchdog timer is shut off.
- IN2 is used to load / start, restart counter.
- If communication is lost, the counter outputs will be set to 0.

Example Hardware Setup for a Repetitive Counter

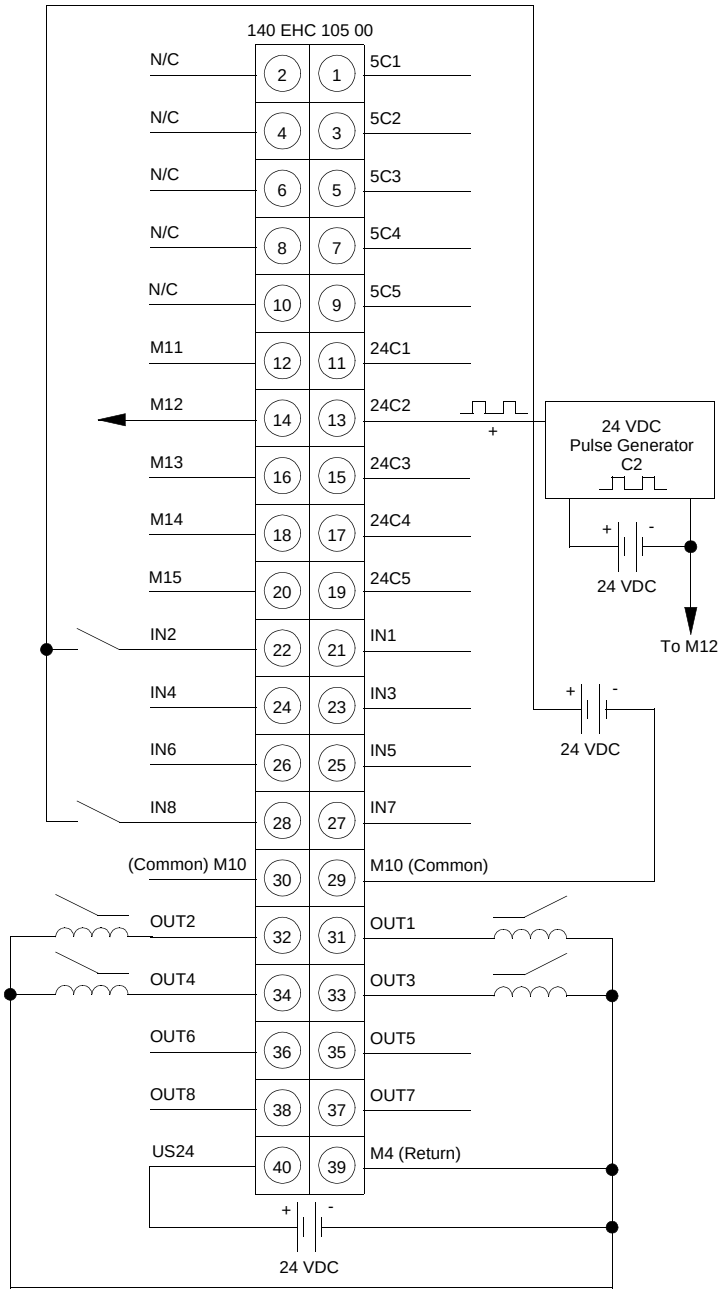
Installation Procedure

For installation follow the steps:

Step	Action
1	Install the EHC 105 00 module into the local backplane's slot 8 and secure it.
2	Install the module terminal strip
3	Connect an external 24 VDC supply voltage (+ pin 40/ pin 39).
4	Connect the pulse input signal to pin 13 (24VDC).
5	Complete the module wiring (see following figure).

Wiring

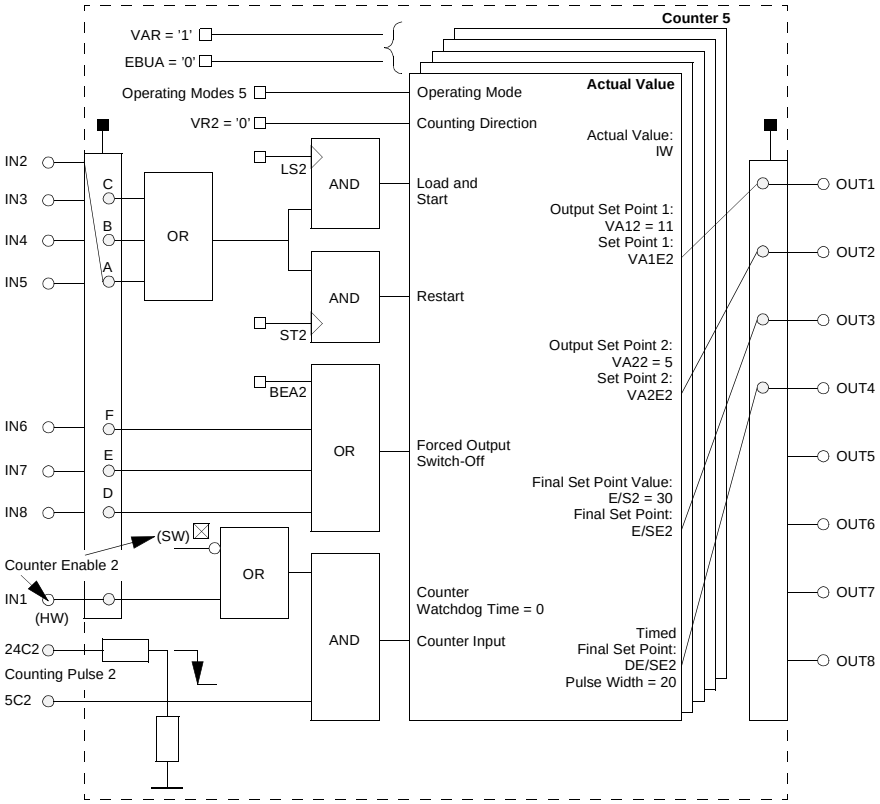
Wiring for repetitive counter:



Example Block Diagram for a Repetitive Counter

Block Diagram

Block Diagram for a repetitive counter with serial set point output activation at mode 5.



	CAUTION
	Risk of configuration failure Do not use outputs OUT1...OUT4 with other counters; such multiple usage is prohibited. **Failure to observe this precaution can result in injury or equipment damage.**

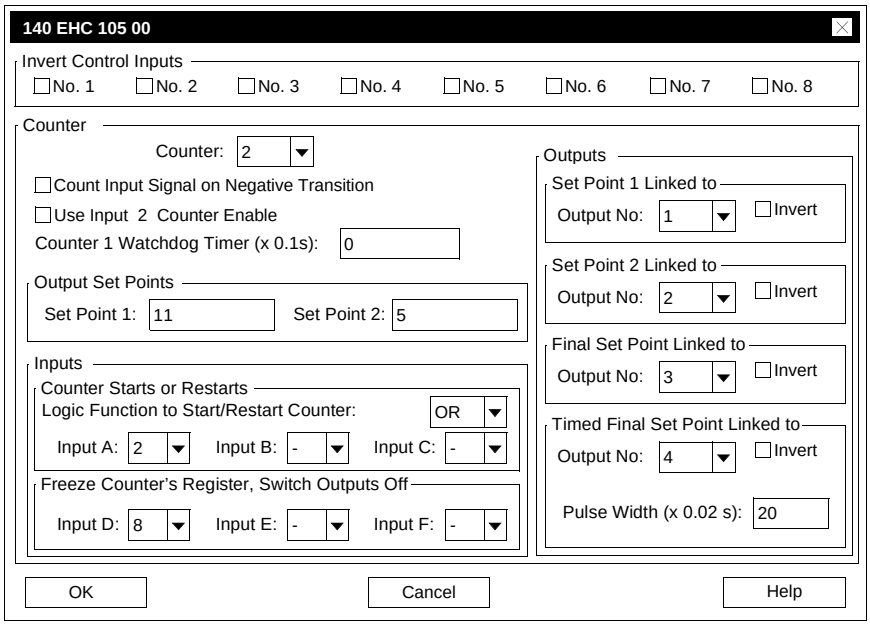
Example Software Settings Using Concept for a Repetitive Counter

Drop Configuration

For the configuration of the module into slot 8 and I/O-Map see *Example Software Settings Using Concept for an Event Counter (Relative), p. 102*.

I/O Configuration Screen

I/O configuration and counter 2 characteristics.



Configuration with the Help of Drop and I/O Configuration Screen for Example Repetitive Counter

Preconditions

Stop the controller before configuring the module.

Configuration Points

Use the following selections to configure the counter specifications within the screens above:

Item	Selections
Counter properties	
Counting pulse 2 with falling edge:	On Negative Transition
Counter Watchdog Time (x0,1s) = 0	Value **0** is selected

Item	Selections
Counter enable assignment to IN2:	**Input No.2 for counter enable** is selected (cross).
Load/start or restart and output switchoff assignments:	
Logic Between Start Inputs: OR.	**OR** is selected.
Enter IN2 as load/start or restart input, no inversion.	**IN2 for Input A:** is selected. No cross at **Invert Control Inputs No.6**.
Enter IN8 as output switchoff, no inversion.	**IN8 for Input D:** is selected. No cross at **Invert Control Inputs No.8**.
Output assignments, features	
Linke Set Point 1 to OUT1 , no inversion.	**Out 1** is selected for Set Point 1. (Multiple usage is prohibited !!) No cross at **Invert**.
Linke Set Point 2 to OUT2 , no inversion.	**Out 2** is selected for Set Point 2. (Multiple usage is prohibited !!) No cross at **Invert**.
Linke Final Set Point to OUT3, no inversion.	**Out 3** is selected for Final Set Point. (Multiple usage is prohibited !!) No cross at **Invert**.
Linke Timed Final Set Point to OUT4, no inversion.	**Out 4** is selected for Timed Final Set Point. (Multiple usage is prohibited !!) No cross at **Invert**.
Timed Final Set Point Pulse Width = 400ms.	Value = **20** is entered for pulse width (x 0,02).
Specify Set Point Values	
Set Point 1 value: 11	Value = **11** is entered.
Set Point 2 value: 5	Value = **5** is entered.
Specify Final Set Point Value; select the 4x... register (see I/O map screen in *Example Software Settings Using Concept for a Repetitive Counter, p. 114*).	
Enter the Final Set Point Value (E/S2=30) as 32bit value (with user program):	E/S2: 400105 = **30 LD** (See output specifications in *Example Specifications for a Repetitive Counter, p. 110*).
Specify counter characteristics:	
Repetitive Counter =0101, Counting up =0000, relative Set Point =0001 (with user program)	**Register 400101 =** 00**5**0hex (See output specifications in *Example Specifications for a Repetitive Counter, p. 110*). **Register 400100 =**00**1**0hex(relative).

Start for Example Repetitive Counter

Starting the Counter

Start the controller, then follow the steps on the module data reference screen:

Step	Action
1	Activate (High) discrete Input 2 (pin 22).
2	Enter LS2 bit in 400101 register (D0 = 1 respectively 0051 hex) (with user program), (See output specifications in *Example Specifications for a Repetitive Counter, p. 110*).

The outputs switch to 1 signal and the counter's actual value is set to 0:

- 300101 register:
  - VA1E2(D1 = OUT1 = 1 signal
  - VA2E2(D9) = OUT2 = 1 signal
- 300100 register:
  - E/SE2(D9) = OUT3 = 0" signal
- 300104 register:
  - counter's actual value = 0

Note: The counter input is inherently enabled, as there has been no discrete input assigned.

Counter 2 counts the pulses at counter input 2:

- At actual value 19 = 30-11 OUT1 switches off and the OUT2 switches on.
- At actual value 25 = 305 OUT2 switches off and the OUT3 switches on.
- At actual value 30 OUT3 switches off and OUT1 switches on.
- The Timed Final Set Point output OUT4 switches on for 400 ms.
- The counters actual value is set to 0.
- The counting procedure repeats.

Switch Off Out1...Out4

The outputs OUT1 .. OUT4 can be switched off:

- with an external 1 signal connected to input IN8 or
- through the 400101 register BEA2 bit (with D2 = 1 respectively 0054 hex, since the operating mode must be retained).

In this case all outputs and the input status word bits (300100 register (D8), 300100register (D9), 300100-register (D1 and D9)) switches to 0 signal. See also *Start and Stop Time Diagram without Hardware Input Configuration, p. 27*.

Restart

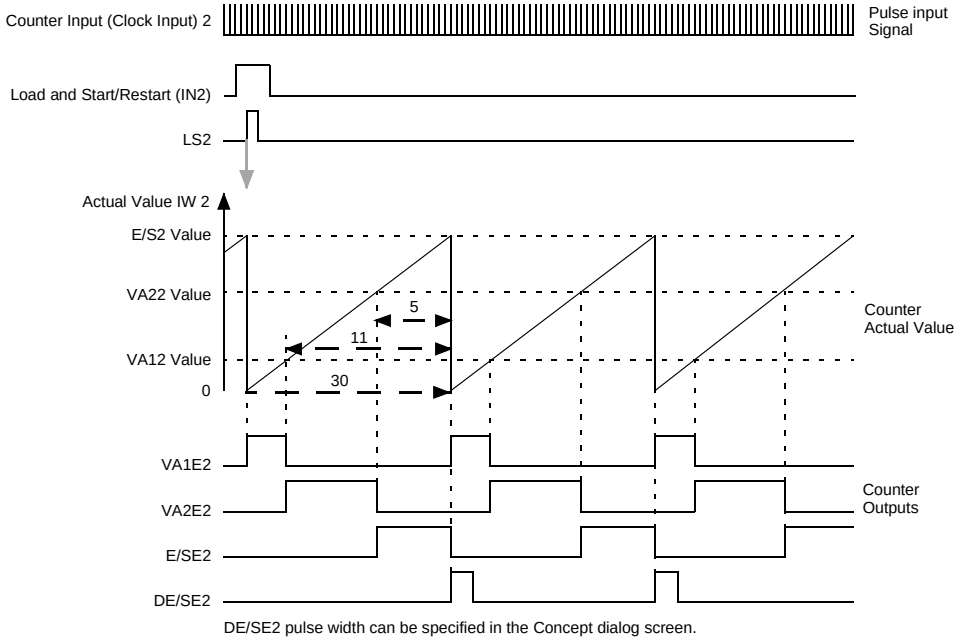
In this example a restart is not possible. There is **no** signification for following conditions:

- 1 signal is activated at input IN2.
- A rising edge at the 400101 register ST2 bit (D1) is entered.

Time Diagram for Example 2, Repetitive Counter

Diagram

Repetitive counter :



Note:

- DE/SE2 pulse width can be specified in the Concept dialog screen.
- The output set points are relative to terminal value E/S2 = 30.
- If the counter's operating mode, counting direction, switch-off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

Configuration Example 3 with Differential Counter

11

At a Glance

Introduction

The following configuration example is valid for the following counter:

- Differential counter, counting down
- Parallel set point output activation
- Counter 3 in mode 3

What's in this Chapter?

This Chapter contains the following Maps:

Configuration Order for Example Differential Counter

Configuration Order

For this example the configuration order is as follows:

- Specifications
- Hardware setup
- Block Diagram for counter
- Software settings using Concept
- Start counter
- Time diagram

Example Specifications for a Differential Counter

Output Specifications

This application describes using counter 3 and 4 as a differential counter with parallel set point output activation, counting down from 30 to 0.
See the following specification for counter 3:

Setpoint (SP)	Linked Outputs	Active Level	Values
FSP (E/SE3)	03	1 -> 0	30 counts (E/S3)
1SP (VA1E3)	01	1 -> 0	11 counts (VA13)
2SP VA2E3)	02	1 -> 0	5 counts (VA23)
TFSP (DE/SE3)	04	0 -> 1 (400 ms)	

Note:

- The values for set points are relative mode.
- For this application the FSP is the starting value for the down counter.
- The differential counter consists of counter 3 and 4. For this application, counter 3 is the master and its configuration also applies to counter 4. The input and output asignements, watchdog time and the set point values for counter 4 were ignored.

Input / Other Specifications

Further specifications:

- Input Pulse is 24 V, not inverted.
- There is no configuration from the forced output switch-off logic to a discrete Input.
- No counter enable comes from discrete input IN3.
- The OR logic for the inputs sets the counter.
- Watchdog timer is shut off.
- There is no input selected using load / start or restart counter.
- If communication is lost, the counter outputs will be set to 0.

Note: For counter 4, only the selections **Invert Counter** and **Input No. 4 for Counter Enable** are usable. All other assignments are ignored.

Example Hardware Setup for a Differential Counter

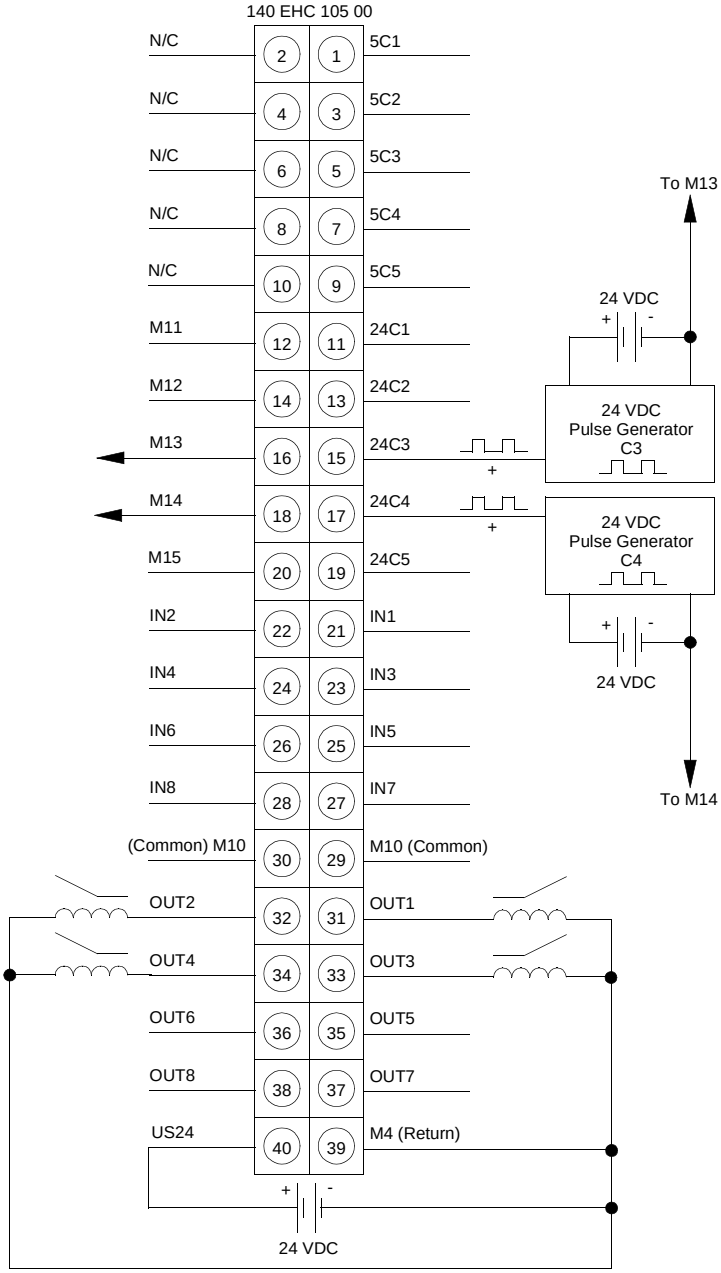
Installation Procedure

For installation follow the steps:

Step	Action
1	Install the EHC 105 00 module into the local backplane's slot 8 and secure it.
2	Install the module terminal strip
3	Connect an external 24 VDC supply voltage (+ pin 40/ pin 39).
4	Connect two counter pulses to pin 15 and 17 (24VDC).
5	Complete the module wiring (see following figure).

Wiring

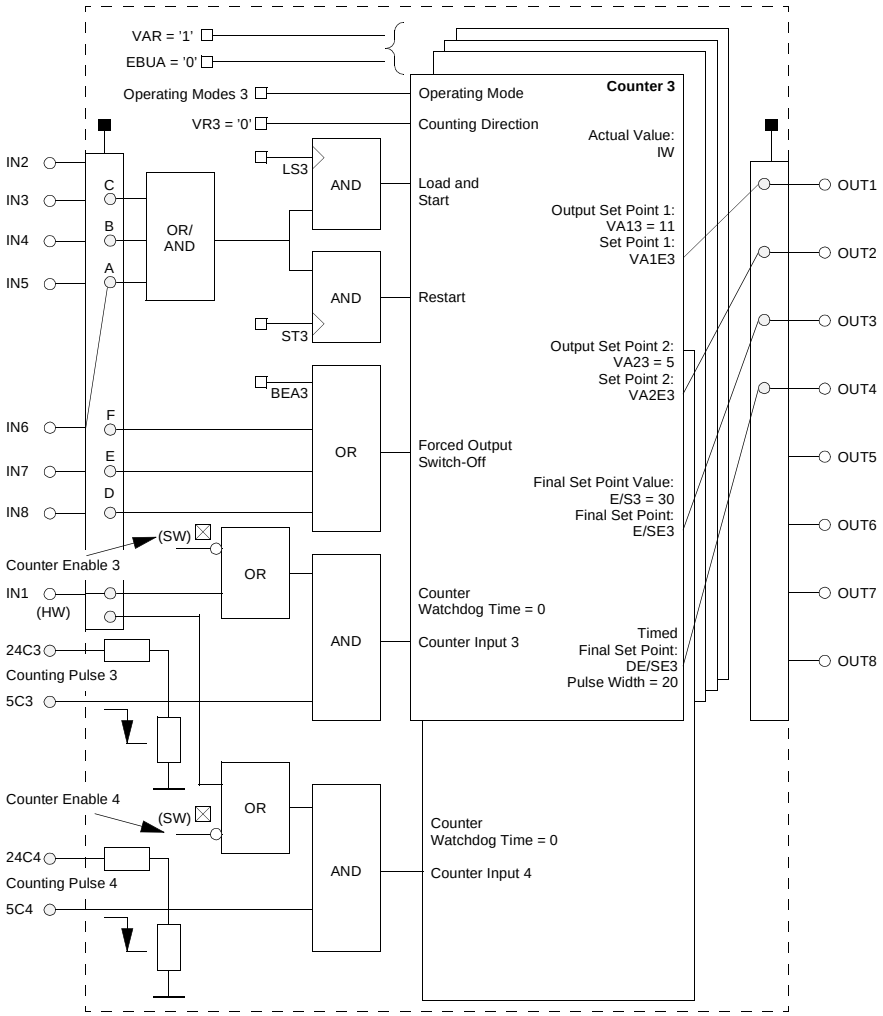
Wiring for differential counter:



Example Block Diagram for a Differential Counter

Block Diagram

Block Diagram for differential counter with parallel set point output activation at mode 3 and counting down.



	CAUTION
	Risk of configuration failure Do not use outputs OUT1...OUT4 with other counters; such multiple usage is prohibited. **Failure to observe this precaution can result in injury or equipment damage.**

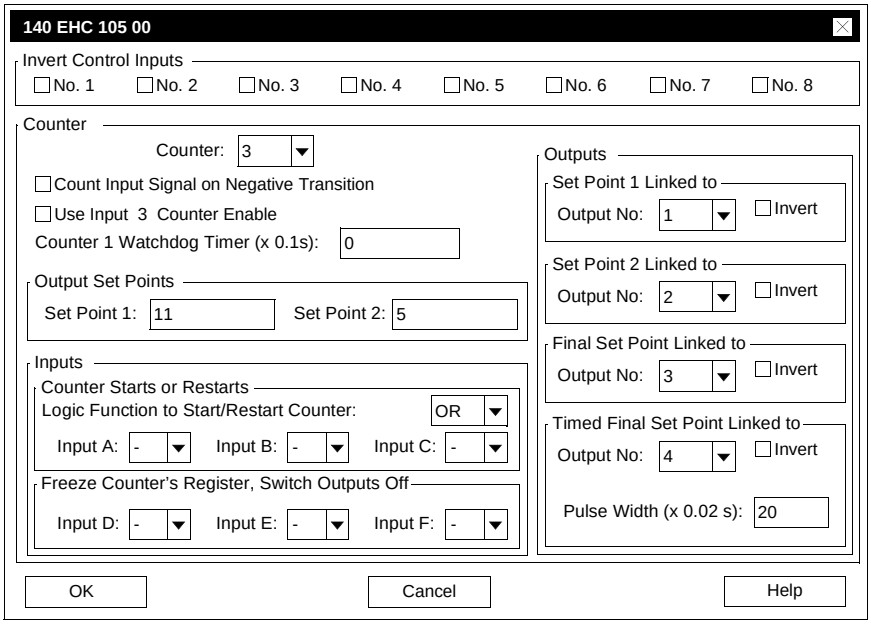
Example Software Settings Using Concept for a Differential Counter

Drop Configuration

For the configuration of the module into slot 8 and I/O-Map see *Example Software Settings Using Concept for an Event Counter (Relative), p. 102*.

I/O Configuration

Screen for I/O configuration and counter 3 characteristics.



Configuration with the Help of Drop and I/O Configuration Screen for Example Differential Counter

Preconditions

Stop the controller before configuring the module.

Configuration Points

Use the following selections to configure the counter specifications within the screens above:

Item	Selections
Counter proberties	
Counting pulse 3 with falling edge:	On Negative Transition
Counter Watchdog Time (x0,1s) = 0	Value 0 is selected.
No counter enable assignment:	No counter enable is selected (no cross).
Load/start or restart and output switchoff assignments:	
Logic Between Start Inputs: OR.	OR is selected.
No input as load/start or restart input.	No INx for Input A is selected.
No input as output switchoff	No INx for Input D is selected.
Output assignments, features	
Linke Set Point 1 to OUT1 , no inversion.	Out 1 is selected for Set Point 1. (Multiple usage is prohibited !!) No cross at InvertInvert.
Linke Set Point 2 to OUT2 , no inversion.	Out 2 is selected for Set Point 2. (Multiple usage is prohibited !!) No cross at Invert.
Linke Final Set Point to OUT3, no inversion.	Out 3 is selected for Final Set Point. (Multiple usage is prohibited !!)No cross at Invert.
Linke Timed Final Set Point to OUT4, no inversion.	Out 4 is selected for Timed Final Set Point. (Multiple usage is prohibited !!) No cross at Invert.
Timed Final Set Point Pulse Width = 400ms.	Value = 20 is entered for Pulse Width (x 0,02).
Specify Set Point Values	
Set Point 1 value: 11	Value = 11 is entered.
Set Point 2 value: 5	Value = 5 is entered.
Specify Final Set Point Value; select the 4x... register (see *Example Software Settings Using Concept for an Event Counter (Relative), p. 102*).	

Item	Selections
Enter the Final Set Point Value (E/S3=30) as 32bit value (with user program):	**E/S3: 400107 = 30 LD** (See output specification in *Example Specifications for a Differential Counter, p. 120*).
Specify counter characteristics:	
Parallel Different Counter =0011, Counting down =1000, relative Set Point =0001 (with user program)	**Register 400101 = 38**00hex (See output specification in *Example Specifications for a Differential Counter, p. 120*.

Start for Example 3, Differential Counter

Counter Steps and Effects

Start the controller and enter LS3 bit in 400101 register (D8 = 1 respectively 3900 hex) (with user program), see output specifications in *Example Specifications for a Differential Counter, p. 120*.
The following effects are appear:

Effect	Description
1	This enables the differential counter.

2	The outputs switch to 1 signal and the counter's actual value is set to 30:
	● 300101 register:
	  ● VA1E3(D2 = OUT1 = 1 signal
	  ● VA2E3(D10) = OUT2 = 1 signal
	● 300100 register:
	  ● E/SE3(D10) = OUT3 = 1 signal
	● 300106 register:
	  ● counter's actual value = 30

3	The pulses for counter 3 counts up and the pulses for counter 4 counts down (Counter pulse input 3 / 4): ● At actual difference value 11 OUT1 switches off. ● At actual difference value 5 OUT2 switches off. ● At actual difference value 0 OUT3 switches off. ● The Timed Final Set Point output OUT4 switches on for 400 ms.

Switch Off Out1...Out4

If the counter has not reached the final set point value, the outputs OUT1 ... OUT4 can be switched off with an 1 signal in the 400101 register BEA3 bit (with D10=1 respectively 3C00hex, since the operating mode must be retained.
In this case all outputs and the input status word bits 300100-register (D10), 300101-register (D2 and D10) switches to 0 signal. See also *Start and Stop Time Diagram without Hardware Input Configuration, p. 27*.

Restart

Note: You can restart only after output switchoff (BEA). See also *Start and Stop Time Diagram without Hardware Input Configuration, p. 27*.

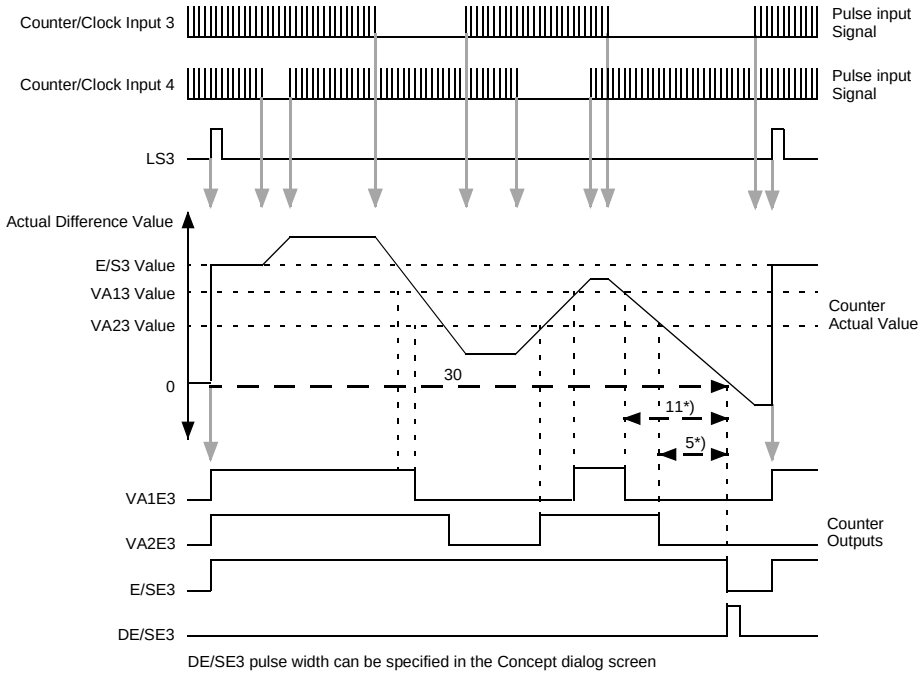
In this example a restart is possible with following conditions:

- The final set point value (actual value 0 in our example) has not been reached.
- A rising edge at the 400101 register ST3 bit (D9, respectively 3A00 hex) is entered.

Load/Start When the counter is reset the counting value is set to 0 and the outputs become active again.

Time Diagram for Example 3, Differential Counter

Time Diagram Differential counter :



DE/SE3 pulse width can be specified in the Concept dialog screen

Note:
- DE/SE2 pulse width can be specified in the Concept dialog screen.
- The output set points are relative to terminal value E/S2 = 30.
- If the counter's operating mode, counting direction, switch-off behavior, or type of set point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

Configuration Example 4 with Event Counter (Absolute)

12

At a Glance

Introduction

The following configuration example is valid for the following counter:

- Event counter, counting up
- Timed set point output activation
- Counter 4 in mode A

What's in this Chapter?

This Chapter contains the following Maps:

Configuration Order for Example Event Counter (Absolute)

Configuration Order

For this example the configuration order is as follows:

- Specifications
- Hardware setup
- Block Diagram for counter
- Software settings using Concept
- Start counter
- Time diagram

Example Specifications for an Event Counter (Absolute)

Output Specifications

This application describes using the counter 4 as an event counter with timed set point output activation, counting up to 30 counts.
Specification for counter 4:

Setpoint (SP)	Linked Outputs	Active Level	Values
FSP (E/SE4)	03	1 -> 0 (s sec)	30 counts (E/S4)
1SP (VA1E4)	01	1 -> 0 (s sec)	11 counts (VA14)
2SP VA2E4)	02	1 -> 0 (s sec)	5 counts (VA24)
TFSP (DE/SE4)	04	0 -> 1 (s sec)	

Note: The values for set points are to configure in absolute mode.

Input / Other Specifications

Further specifications:

- Input pulse is 24 V, not inverted.
- A field signal is connected to input 8 and forces output switchoff.
- IN4 is selected to enable the counter.
- The OR logic for the inputs sets the counter.
- Watchdog timer is shut off.
- IN7 is used to load / start, restart counter.
- If communication is lost, the counter outputs will be set to 0.

Example Hardware Set up for an Event Counter (Absolute)

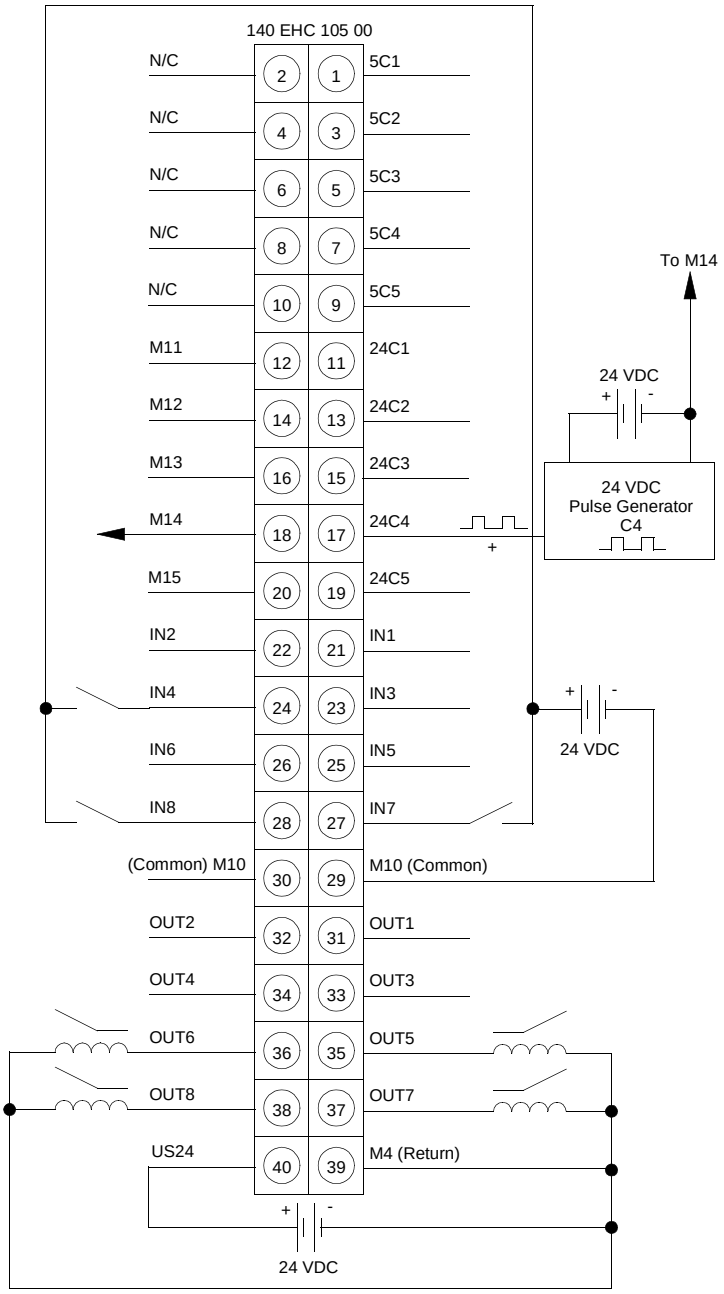
Installation Procedure

For installation follow the steps:

Step	Action
1	Install the EHC 105 00 module into the local backplane's slot 8 and secure it.
2	Install the module terminal strip
3	Connect an external 24 VDC supply voltage (+ pin 40/ pin 39).
4	Connect the Pulse input signal to pin 17 (24VDC).
5	Complete the module wiring (see next figure).

Wiring

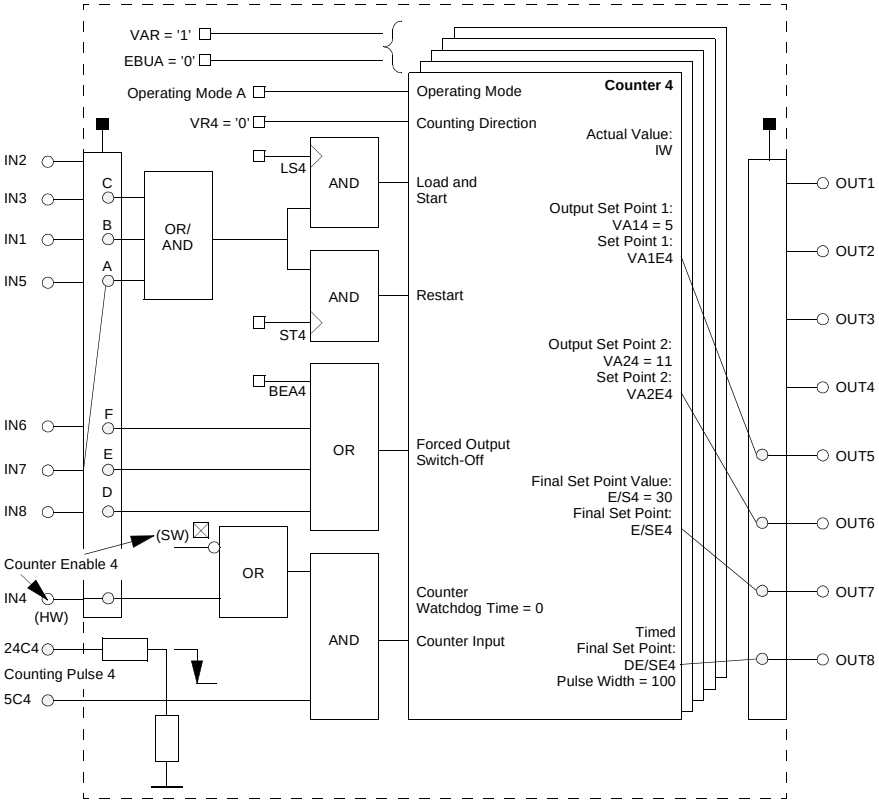
Wiring for event counter (absolute):



Example Block Diagram for an Event Counter (Absolute)

Block Diagram

Block Diagram for event counter with serial set point output activation at mode 5.



	CAUTION
	Risk of configuration failure Do not use outputs OUT1...OUT4 with other counters, as such multiple useage is prohibited. **Failure to observe this precaution can result in injury or equipment damage.**

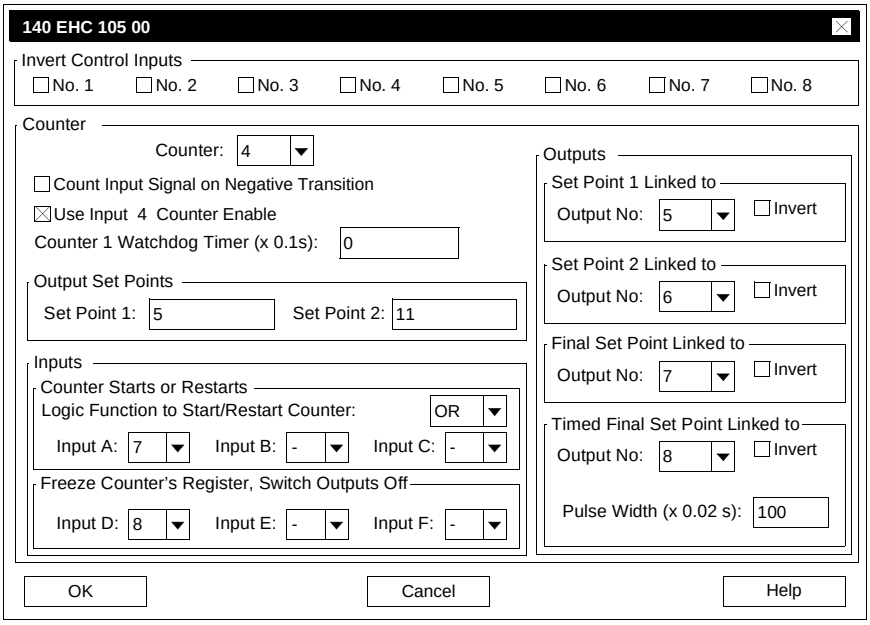
Example Software Settings Using Concept for an Event Counter (Absolute)

Drop Configuration

For the configuration of the module into slot 8 and I/O-Map see *Example Software Settings Using Concept for an Event Counter (Relative), p. 102*.

I/O Configuration

I/O configuration and counter 4 characteristics:



Configuration with the Help of Drop and I/O Configuration Screen for Example Event Counter (Absolute)

Preconditions

Stop the controller before configuring the module.

Configuration

Use the following selections to configure the counter specifications within the screens above.:

Items	Selections
Counter proberties	
Counting pulse 4 with falling edge:	On Negative Transition
Counter Watchdog Time (x0,1s) = 0	Value 0 is selected.

Items	Selections
Counter enable assignment to IN4:	Input No.4 for counter enable is selected (cross).
Load/start or restart and output switchoff assignments:	
Logic Between Start Inputs: OR.	OR is selected.
Enter IN7 as load/start or restart input, no inversion.	IN7 for Input A: is selected. No cross at "Invert Control Inputs No.6".
Enter IN8 as output switchoff, no inversion.	IN8 for Input D: is selected. No cross at "Invert Control Inputs No.8".
Output assignments, features	
Linke Set Point 1 to OUT5 , no inversion.	Out 5 is selected for Set Point 1. (Multiple usage is prohibited !!) No cross at Invert.
Linke Set Point 2 to OUT6 , no inversion.	Out 6 is selected for Set Point 2. (Multiple usage is prohibited !!) No cross at Invert.
Linke Final Set Point to OUT7, no inversion.	Out 7 is selected for Final Set Point. (Multiple usage is prohibited !!)No cross at Invert.
Linke Timed Final Set Point to OUT8, no inversion.	Out 8 is selected for Timed Final Set Point. (Multiple usage is prohibited !!) No cross at Invert.
Timed Final Set Point Pulse Width = 2 sec	Value = 100 is entered for Pulse Width (x 0,02).
Specify Set Point Values	
Set Point 1 value: 11	Value = 11 is entered.
Set Point 2 value: 5	Value = 5 is entered.
Specify Final Set Point Value; select the 4x... register (see *Example Software Settings Using Concept for an Event Counter (Relative), p. 102*).	
Enter the Final Set Point Value (E/S2=30) as 32bit value (with user program):	E/S4: 400109 = 30 LD (See output specification in *Example Specifications for an Event Counter (Absolute), p. 130*).
Specify counter characteristics:	
Parallel timend Event Counter =1010, Counting up =0000, absolute Set Point =0000 (with user program)	Register 400102 = 00A0hex (See output specification in *Example Specifications for an Event Counter (Absolute), p. 130*)

Start for Example Event Counter (Absolute)

Load/start the counter

Start the controller, then follow the steps on the module data reference screen:

Step	Action
1	Activate (High) discrete Input 7 (pin 27).
2	Enter LS4 bit in 400102 register (D0 = 1 respectively 00A1 hex) (with user program), (See output specification in *Example Specifications for an Event Counter (Absolute), p. 130*).

The outputs switch to 1 signal and the counter's actual value is set to 0:

- 300101 register:
  - VA1E4 (D3) = 1 signal
  - VA2E4 (D11) = 1 signal
- 300100 - register:
  - E/SE4 (D11) = 1 signal
- All outputs switches off (Out 5, 6, 7, 8).
- counter's actual value = 0

Enabling counter 1

Activate (High) discrete Input IN4 (pin 24, counter enable):

Effect	Description
1	Counter 4 counts the pulses at counter input 4: ● At actual value 5, OUT5 switches on for 2 sec. ● At actual value 11, OUT6 switches on for 2 sec. ● At actual value 30, OUT7 switches on for 2 sec. ● The Timed Final Set Point output OUT8 switches on for 2 sec.
2	The register signals from counter 4 have following states: ● At actual value 5 = VA1E4 switches off. ● At actual value 11 = VA2E4 switches off. ● At actual value 30 = E/SE4 switches off.

Switch Off Out1...Out4

If the counter has not reached the final set point value, the outputs OUT5 .. OUT8 can be switched off:

- with an external 1 signal connected to input IN8 or
- through the 400102 register BEA4 bit (with D2 = 1 respectively 00A4 hex, since the operating mode must be retained).

In this case all outputs and the input status word bits (300100 register (D11), 300101register (D3 and D11)) switche to 0 signal. See also time diagrams beginning with *Start and Stop Time Diagram without Hardware Input Configuration, p. 27*.

Restart

Note: You can restart only after output switchoff (BEA). See also time diagrams beginning with*Start and Stop Time Diagram without Hardware Input Configuration, p. 27*.

In this example a restart is possible with following conditions:

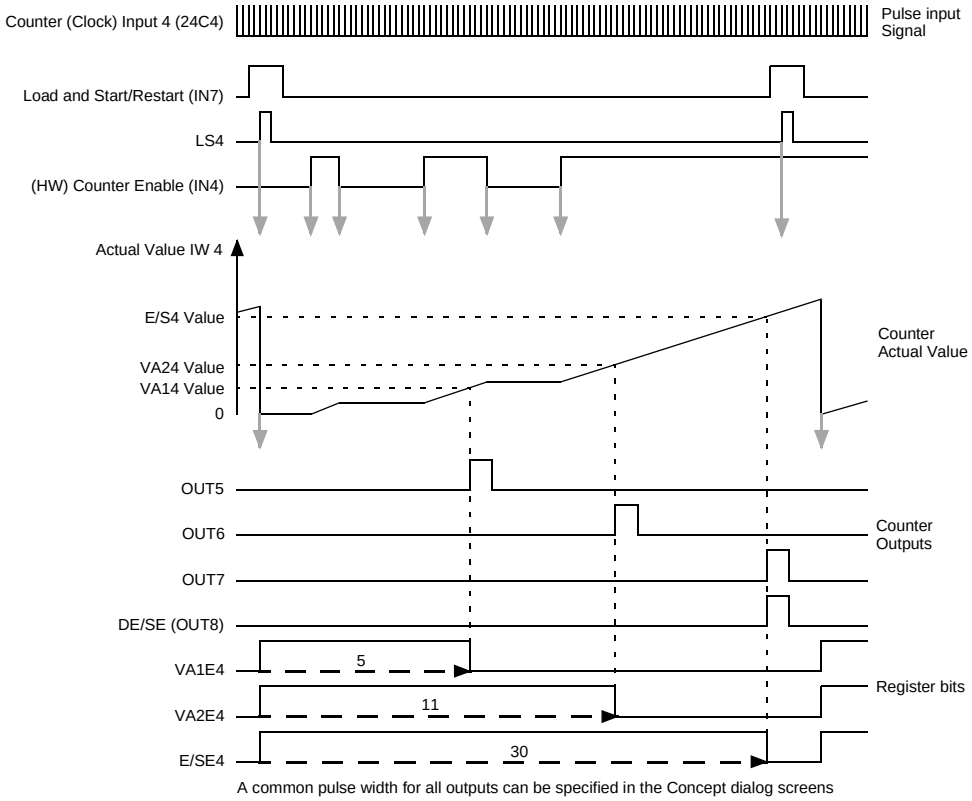
- The final set point value (actual value 30 in our example) has not been reached.
- High signal is activated at input IN7.
- A rising edge at the 400102 register ST4 bit (D1, respectively 00A1 hex) is entered.

Load/Start

When the counter is reset the counting value is set to 0 and the outputs became active again.

Example Time Diagram for an Event Counter (Absolute)

Time Diagram Event counter (absolute and counting up) :



Note:
If the counter's operating mode, counting direction, switch-off behavior, or type of set point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

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